A Differential Active Load and its Applications in CMOS Analog Circuit Designs

Vladimir I. Prodanov, *Student Member, IEEE*, and Michael M. Green, *Member, IEEE*

***Abstract*—In this paper we describe a CMOS *differential active load* and show how it can be used to create various useful structures. Tunable current gain stages and current squaring circuits are discussed. Their connection to a differential pair-based transconductor results in broad-range tunable transconductor structures suitable for adaptive continuous-time filtering applications and a four-quadrant voltage multiplier.**

***Index Terms*— Analog multipliers, CMOS analog integrated circuits, transconductors, tunable filters.**

I. Introduction

ANALOG continuous-time filters are an important part of both analog and mixed-mode signal processors. Monolithic analog filters are often made to be electronically tunable to allow for "trimming," that is, to make small changes in the filter's frequency response. This is needed in order to compensate for the effects that process variations, temperature and aging have on the filter's critical frequencies. Normally, a tunability range of an octave is sufficient for this purpose alone and can easily be accomplished in both CMOS and bipolar technology.

In many situations, however, certain "optimal" filtering, based on the frequency spectrum of the input signal, is desired. An example which will be expanded upon later in this paper is the decoding of barcode signals in the presence of noise for different distances to the barcode label and different barcode densities. In this case, tunability on the order of a decade is required because a significant variability in the bandwidth of the input signal must be taken into account along with the usual circuit parameter variations.

An area where an even broader tuning range can be required is the prefiltering in general-purpose signal processors. For this reason discrete-time circuits (e.g., switched-capacitor or switched-current) are used to allow an even larger tuning range via an external clock reference.

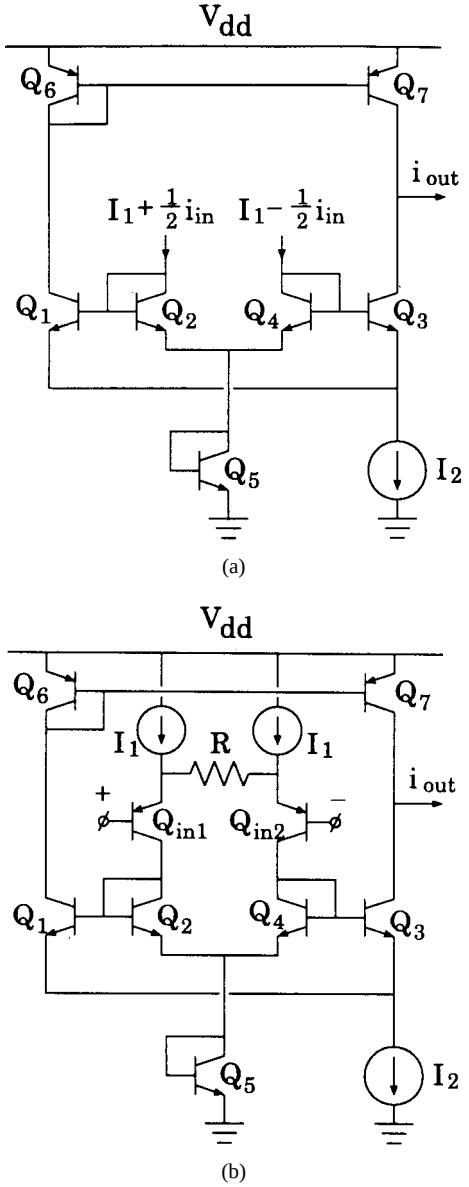


Fig. 1. Tunable bipolar structures. (a) Current amplifier. (b) Linear transconductor.

In this paper we will focus our attention on continuous-time filtering using CMOS circuitry where the goal is to allow as large a tuning range as possible. When using g_m–C filtering for this purpose, the use of a BJT process is often

Manuscript received September 6, 1995; revised December 8, 1995. This paper was recommended by Associate Editor L. A. Akers.

V. I. Prodanov is with the Department of Electrical Engineering, College of Engineering and Applied Sciences, State University of New York, Stony Brook, NY 11794 USA.

M. M. Green was with the Department of Electrical Engineering, College of Engineering and Applied Sciences, State University of New York, Stony Brook, NY 11794 USA. He is now with the Department of Electrical and Computer Engineering, University of California, Irvine, CA 92697 USA.

Publisher Item Identifier S 1057-7130(97)02005-3.

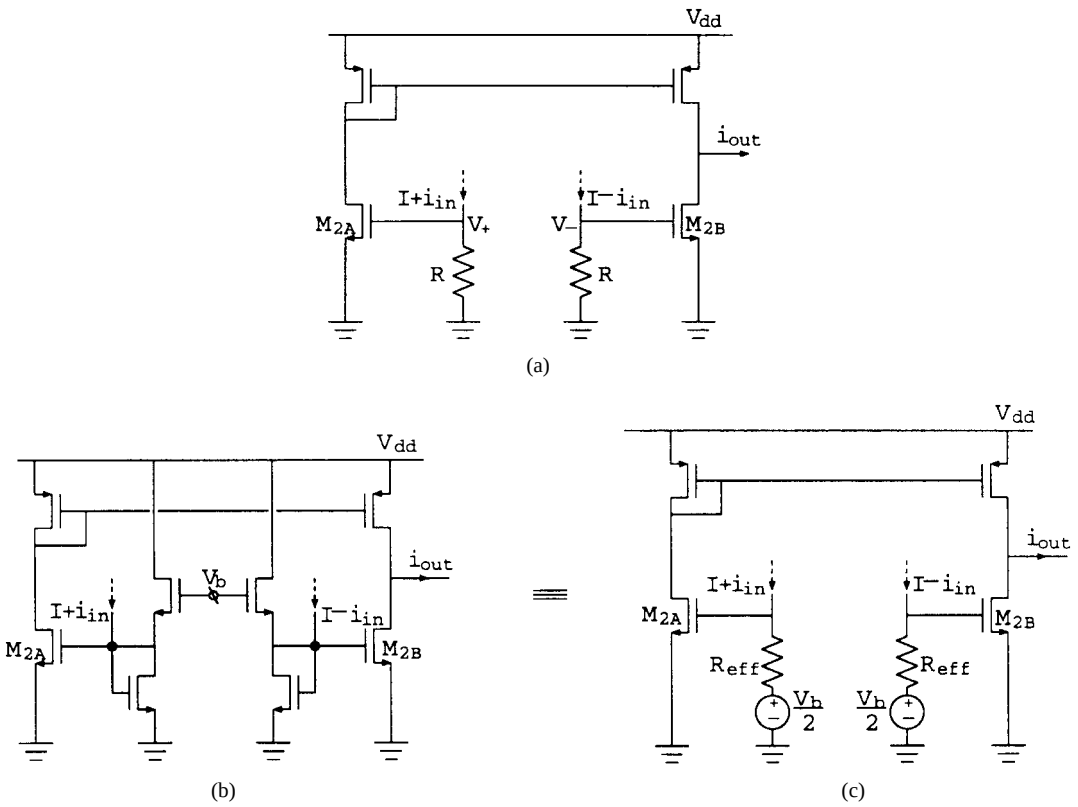


Fig. 2. Current gain stages: (a) with passive resistors; (b) with all-MOS linear i-to-v converters; (c) equivalent circuit for (b).

preferable to a CMOS process for a number of reasons. First, the translinear principle [9], which exploits the exponential characteristic of the base-emitter voltage versus the collector current, allows elegant structures such as the Gilbert gain cell that have a very large linear range. Second, since the g_m of a BJT is proportional to its dc collector current, these circuits can have a very large tuning range. A typical member of this circuit family is the β-immune type "A" cell [9]. Fig. 1(a) shows an "A" cell-based BJT current amplifier whose gain $(A_i = \frac{1}{2}(I_2/I_1))$ can be tuned in a range exceeding a decade by varying the tail current. In Fig. 1(b) a broad-range tunable BJT transconductor is shown, which results from cascading a fixed-value linear transconductor with the Fig. 1(a) tunable current gain stage.

On the other hand, since the g_m of a saturated MOS transistor is proportional to the square root of its dc drain current, one must quadruple the bias current of any transconductance circuit based on transistors in saturation (such as the MOS differential pair), in order to double its g_m. This problem is exacerbated when the circuit is operated from low supply voltages by the fact that any increase in g_m achieved by increasing the drain current is accompanied by a proportional increase in the transistor's $V_{GS} - V_t$. Circuits based on an MOS transistor biased in its triode region with the gate voltage tuned are also very common and in general can have a broader tuning range. Unfortunately, when the supply voltages are scaled down to 3 V this range is significantly reduced. Hence, achieving an acceptable tuning range for adaptive filtering applications in reduced feature-size CMOS technology is becoming extremely difficult. One alternative, suggested in [1], is to make the capacitors tunable instead of the resistive elements. The disadvantage of this method is that the tuning range is limited to an octave and significant current overhead is required.

In this paper we investigate the possibility for increasing the tuning range of CMOS transconductors by cascading a class-A CMOS tunable transconductor and tunable current gain stage. As mentioned in the beginning of this introduction the two-stage idea is the cornerstone in designing tunable bipolar transconductors (e.g., Fig. 1(b)); however, we believe the work presented here is the first to consider the possibility for its CMOS implementation. In the next section the realization of an MOS tunable current gain stage is discussed. To guarantee its robust operation a new circuit called the Differential Active Load (DAL) is developed. In Section III broad-range tunable CMOS transconductors based on the previously developed current gain stage are introduced. In Section IV the measured results from a fifth-order decade-tunable g_m–C pulse-shaping filter designed for barcode scanning applications are used to illustrate the various properties of the proposed two-stage broad-range tunable transconductance blocks. Finally, in Section V two additional (nonfiltering) applications of the DAL circuit are described. In particular the implementation of a current squaring circuit and a CMOS four-quadrant multiplier are considered.

II. CMOS Tunable Current-Gain Stage and Differential Active Load

To realize the two-stage idea, a suitable CMOS current gain stage must first be developed. We begin our derivation

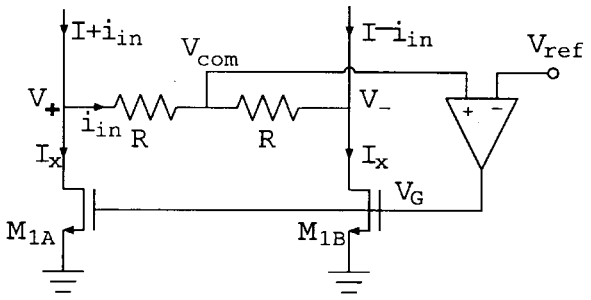


Fig. 3. Differential output *I–V* converter with common-mode feedback.

by identifying some general characteristics of current gain stages.

In the Fig. 1(a) circuit, transistors Q_2, Q_4 and Q_5 act as a simple current-to-voltage converter, with $i_{\rm in}$ as the input current and the voltages on the bases of Q_2 and Q_4 as the output. Transistors Q_1, Q_3, Q_6, and Q_7 act as a voltage-to-current converter with the Q_2 and Q_4 base voltages as the inputs and $i_{\rm out}$ as the output. Although each individual conversion is nonlinear, the translinear principle dictates that their composite is linear, hence $i_{\rm out}$ is proportional to $i_{\rm in}$. We now take the same general approach using MOS transistors. In the Fig. 2(a) circuit, the resistors realize an elementary i-to-v converter and transistors M_{2A} and M_{2B} realize the v-to-i converter, which has the following characteristic:

$$i_{\rm out} = \beta_2 (V_+ - V_-)\left(\frac{V_+ + V_-}{2} - V_t\right). \tag{1}$$

The above equation is the basis of many circuits which use saturated MOS transistors [2], [7] because under the condition of balanced input voltages, where $V_{\rm com} \equiv (V_+ + V_-)/2$ is a constant, (1) describes a linear v–i conversion.

The use of the two resistors in Fig. 2(a) does realize the balanced input voltages constraint so that $V_{\rm com}$ is indeed constant. However, to produce sufficient turn-on (common-mode) voltages, resistors and/or bias currents I with excessive values must be used. In addition, because these dc voltages are linearly dependent on the bias current I they can not provide the robust common-mode biasing required by $M_{2A,B}$.

The need for large value resistors and tail currents can be eliminated by replacing the passive R's with the all-MOS linear i-to-v converter [2] as shown in Fig. 2(b). However, the sensitivity of V_+ and V_- to I will still be present (see its equivalent circuit in Fig. 2(c)).

The standard way of solving such common-mode problems is by use of a common-mode feedback structure (e.g., Fig. 3). The common-mode feedback (cmfb) amplifier senses the difference $V_{\rm com} - V_{\rm ref}$ and adjusts I_x appropriately to null this difference. Thus if the gain of the cmfb amplifier is high $V_{\rm com}$ is kept constant (equal to $V_{\rm ref}$), independent of I.

A similar common-mode stabilization effect can be achieved even if the cmfb amplifier is omitted simply by connecting $V_{\rm com}$ directly to V_G. The resulting structure, called the differential active load (DAL), is shown in Fig. 4(a). As in

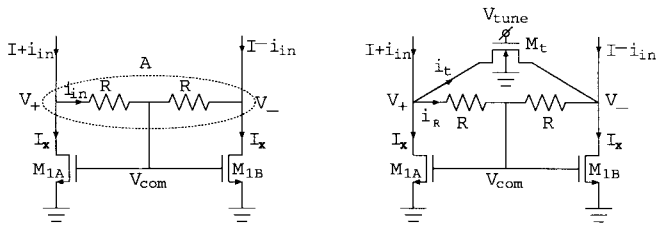


Fig. 4. Differential active loads (DAL). (a) Simple. (b) Voltage tuning.

the common-mode feedback topology, it performs current-to-voltage conversion, where transistors M_{1A} and M_{1B} conduct only dc (common-mode) current and the resistors conduct only differential current. The operation of this circuit is as follows: Since transistors M_{1A} and M_{1B} are in saturation and their gates are tied together, their drain currents I_x must be the same. To find I_x one writes the following KCL equation for supernode "A":

$$I + i_{\rm in} + I - i_{\rm in} = 2I_x \tag{2}$$

which simplifies to

$$I_x = I. \tag{3}$$

Since I_x is independent of small-signal current $i_{\rm in}$, the gate node $V_{\rm com}$ is a small-signal ground.

Now we can express the output voltages V_+ and V_- of the current-to-voltage converter in terms of $R, V_{\rm com}$ and the input current $i_{\rm in}$:

$$\begin{aligned} V_+ &= V_{\rm com} + Ri_{\rm in} \\ V_- &= V_{\rm com} - Ri_{\rm in} \end{aligned} \tag{4}$$

or, equivalently

$$v_d \equiv V_+ - V_- = 2Ri_{\rm in} \tag{5}$$

$$V_{\rm com} = \frac{1}{2}(V_+ + V_-) = \sqrt{\frac{2I}{\beta_1}} + V_t. \tag{6}$$

As it can be seen from the above two equations the DAL treats the differential and common-mode signals differently. The differential input current $i_{\rm in}$ is converted linearly to a differential voltage v_d, whereas the common-mode current I is converted in square-root fashion to a common-mode voltage $V_{\rm com}$. Hence, the circuit can perform both linear current-to-voltage conversion and deliver a robust common-mode biasing provided it is driven by a transconductance block with a reasonably high CMRR over the desired frequency range. In addition, since the value of R affects only the differential voltage v_d and not the common-mode voltage $V_{\rm com}$, a tunable DAL can be implemented if R is made electronically adjustable.

The circuit in Fig. 4(b) is a voltage tunable DAL. As in the Fig. 4(a) circuit the dc current I is conducted by M_{1A} and M_{1B} whereas the ac current $i_{\rm in}$ is split between the resistors and triode-region transistor M_t, i.e.,

$$i_{\rm in} = i_R + i_t \tag{7}$$

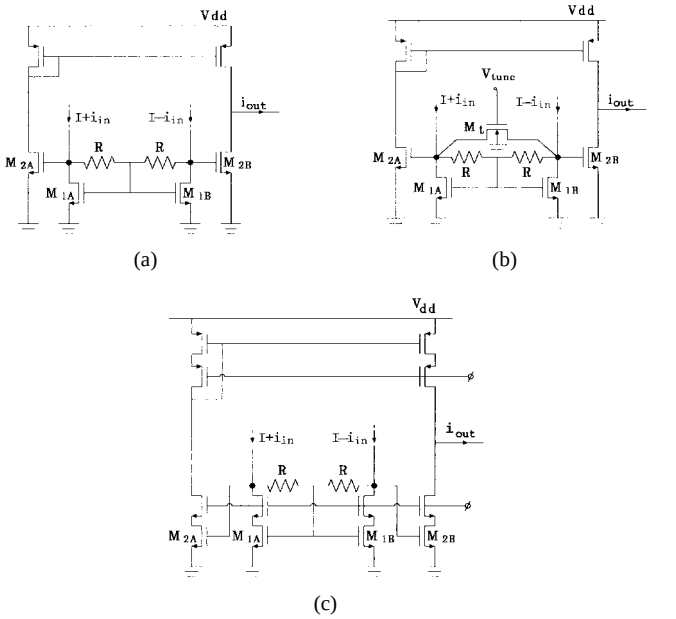


Fig. 5. MOS Current Gain Stages. (a) Simple. (b) Voltage tunable. (c) With increased output resistance.

where

$$i_R = \frac{1}{2R}(V_+ - V_-) \tag{8}$$

$$i_t = \beta_t\left[V_{\text{tune}} - V_t - \frac{V_+ + V_-}{2}\right](V_+ - V_-)$$
$$= \beta_t[V_{\text{tune}} - V_t - V_{\text{com}}](V_+ - V_-). \tag{9}$$

The last equation indicates that under first-order analysis M_t does not affect the linearity of the circuit. To see how the circuit can be tuned we substitute the expressions for i_R and i_t back into (7). After rearrangement we have:

$$V_d \equiv V_+ - V_- = 2R_{\text{eff}} i_{\text{in}} \tag{10}$$

which has the same form as (5) but instead of the fixed value resistor R we have a voltage tunable one with value:

$$R_{\text{eff}} = \frac{R}{1 + 2\beta_t R(V_{\text{tune}} - V_t - V_{\text{com}})}. \tag{11}$$

If the passive resistors in Fig. 2(a) are replaced by the DAL, the Fig. 5 current gain stages result. It is straightforward to show that for the Fig. 5(a) circuit the following input-output current relation holds:

$$i_{\text{out}} = A_i i_{\text{in}} \tag{12}$$

where A_i denotes the current gain of the circuit and is given by

$$A_i = 2R\beta_2(V_{\text{com}} - V_t) = 2R\beta_2\left(\sqrt{\frac{2}{\beta_1}I}\right). \tag{13}$$

Since for proper operation all transistors must remain in saturation, the above equation is subject to the following constraint:

$$Ri_{\text{in(max)}} < \min\left\{V_t, \sqrt{\frac{I}{\beta_1}}\right\}. \tag{14}$$

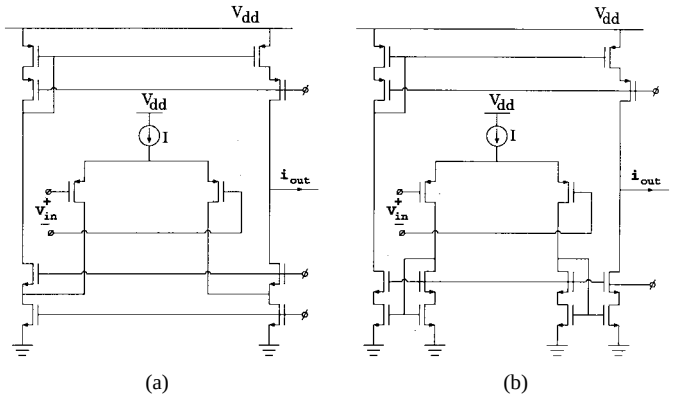


Fig. 6. Simple CMOS Transconductors with (a) folded cascode output stage and (b) three–mirror output stage.

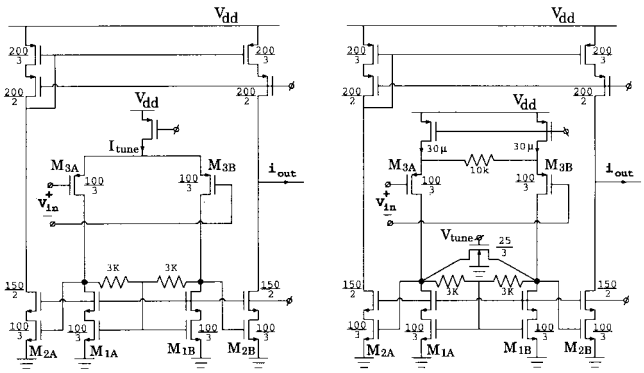


Fig. 7. Broad range tunable CMOS transconductors: (a) with g_m proportional to tail current and (b) based on voltage tunable CGS.

The relation governing the voltage tunable DAL-based circuit shown in Fig. 5(b) can be obtained from the one given for the DAL-based circuit by simply replacing R by R_{eff}.

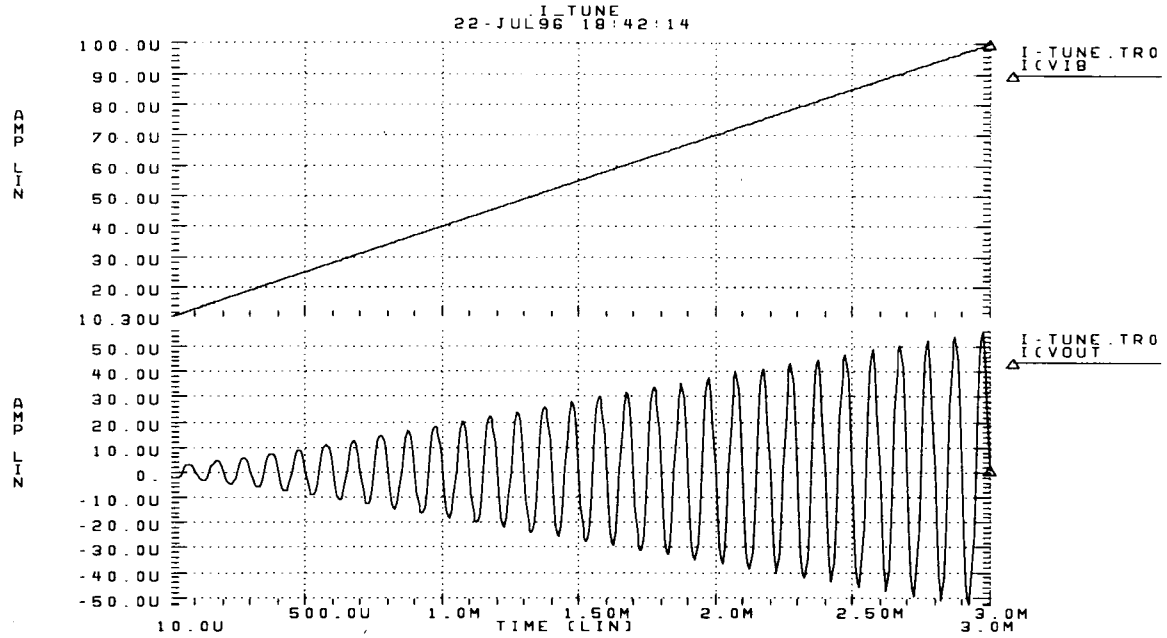
It should be noted that in both cases the resulting current gain stages can be tuned in a square root fashion by varying the dc current I (see (13)). This property will be used in the next section to design a differential pair-based transconductance block with its g_m proportional to its tail current.

In addition, by changing V_{tune} for the voltage-tunable DAL case broad-range tuning is possible. In this case the biasing currents are constant, and so is the power dissipation. The achievable tuning factor M is given by

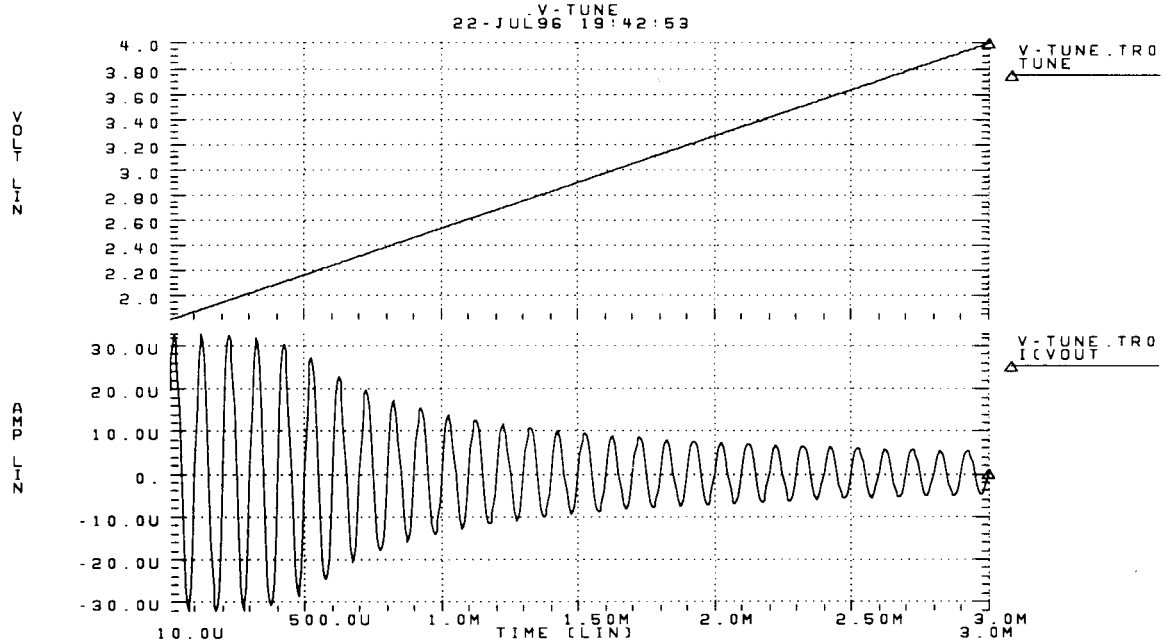
$$M = \frac{R_{\text{eff(max)}}}{R_{\text{eff(min)}}} = \frac{R}{R_{\text{eff(min)}}}$$
$$= 1 + 2\beta_{M_t} R(V_{\text{tune(max)}} - V_t - V_{\text{com}}). \tag{15}$$

For reasonable size resistors and transistors with $V_t = .75 \sim .8$ V and single supply voltage of 5 V, M is in the order of 10.

For most applications it will be beneficial that the output resistance of the designed current gain stages have value beyond that of a single transistor. This can be accomplished, without significant reduction in the allowable output swing in a way very similar to the one employed in designing high-swing CMOS current mirrors (e.g., Fig. 5(c)).



(a)



(b)

Fig. 8. Simulated modulation characteristics of (a) Fig. 7(a) transconductor and (b) Fig. 7(b) transconductor.

III. Broad-Range Tunable CMOS Transconductors

Modifications of the simple long-tail MOS differential pair are commonly used in the design of linearized transconductance elements employed in continuous-time g_m–C filters [4], [8], [10]. The folded-cascode configuration (e.g., Fig. 6(a)) or the standard three-mirror configuration (Fig. 6(b)) are generally preferred for circuit blocks where high output swing is required.

Each of those two configurations can be directly replaced by the developed Fig. 5 current gain stages. Two such cascades of a differential pair input stage and a current gain stage are shown in Fig. 7. The effective transconductance $g_{m(\text{eff})}$ of both circuits is of the form:

$$g_{m(\text{eff})} = g_{m3}A_i \tag{16}$$

where A_i is the gain of the CGS.

Since both g_{m3} and A_i of the Fig. 7(a) circuit are proportional to the square root of the biasing current I, the effective overall transconductance $g_{m(\text{eff})}$ is proportional to I itself and given by

$$g_{m(\text{eff})} = g_{m3}A_i = 2R\beta_2\sqrt{\frac{\beta_3}{\beta_1}}I. \tag{17}$$

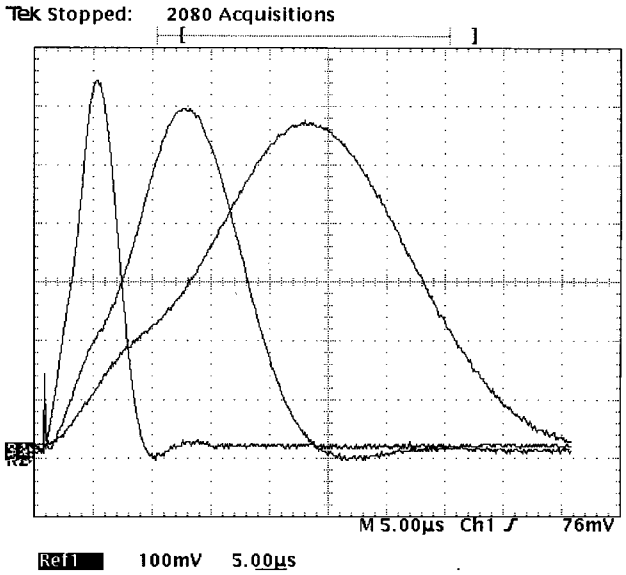


Fig. 9. Oscilloscope plots showing step response for three different tuning voltages.

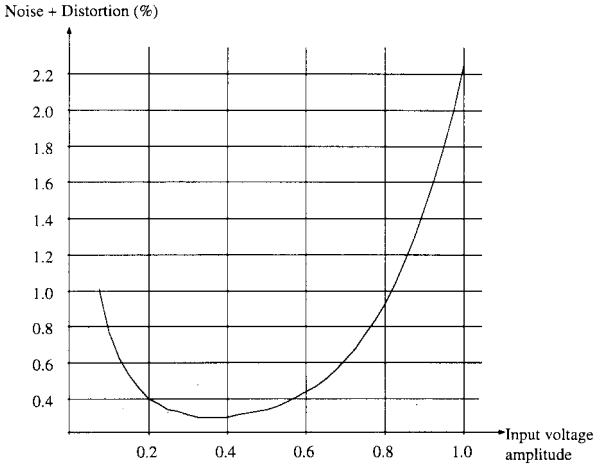


Fig. 10. Noise + distortion versus input amplitude.

Since the Fig. 7(a) circuit exhibits a transconductance proportional to the bias current it can be used efficiently in such applications as the design of artificial CMOS neural networks [3] where power dissipation must be kept low and broad-range tunability is needed.

Note that the price paid for the increase in the tuning range in terms of headroom reduction is minimal, because both the input and the output voltage requirements of the developed current gain stages are the same as those of the three-mirror circuit.

In Fig. 7(b) source degeneration is used to increase the transconductance block's linear range. Unfortunately the degeneration leads to a nearly fixed differential pair transconductance of approximately $1/R_d$. As a result $g_{m(\text{eff})}$ can be varied only by varying A_i, hence in square root fashion with I. To increase the tuning range of this circuit a voltage-tunable CGS is used instead.

Both Fig. 7 circuits were simulated using BSIM (level 13) models provided for the MOSIS 2 μm orbit analog process.

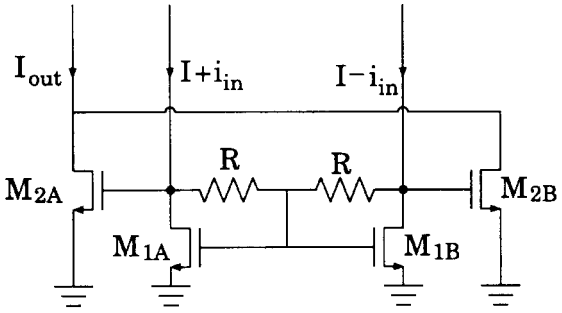


Fig. 11. Differential-input current-squaring circuit.

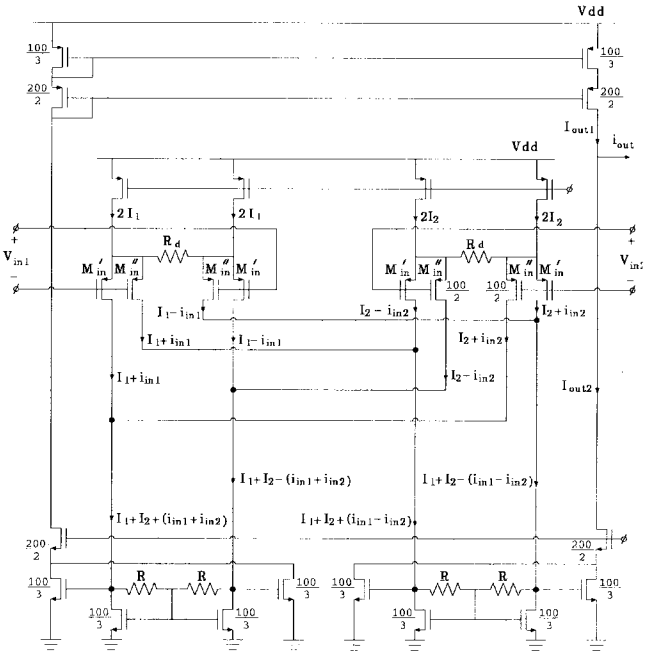


Fig. 12. Full schematic of four-quadrant quarter-square multiplier.

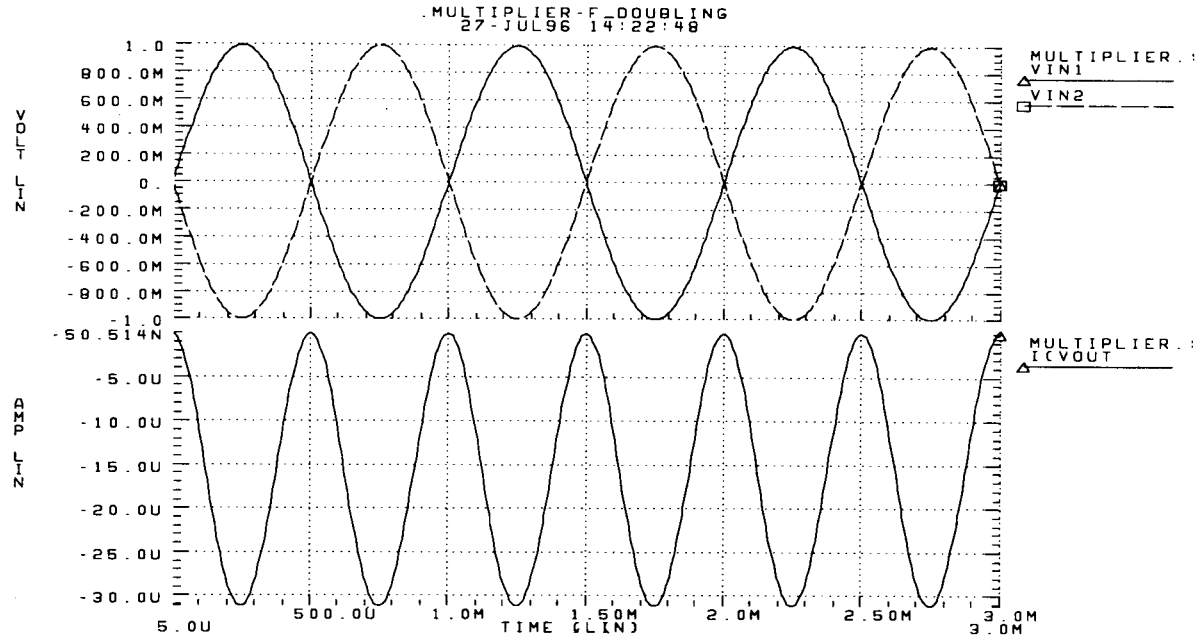
Fig. 8 shows their modulation characteristics—that is, their output currents as a function of the tuning current/voltage when the input is driven by a sine wave.

IV. Experimental Results

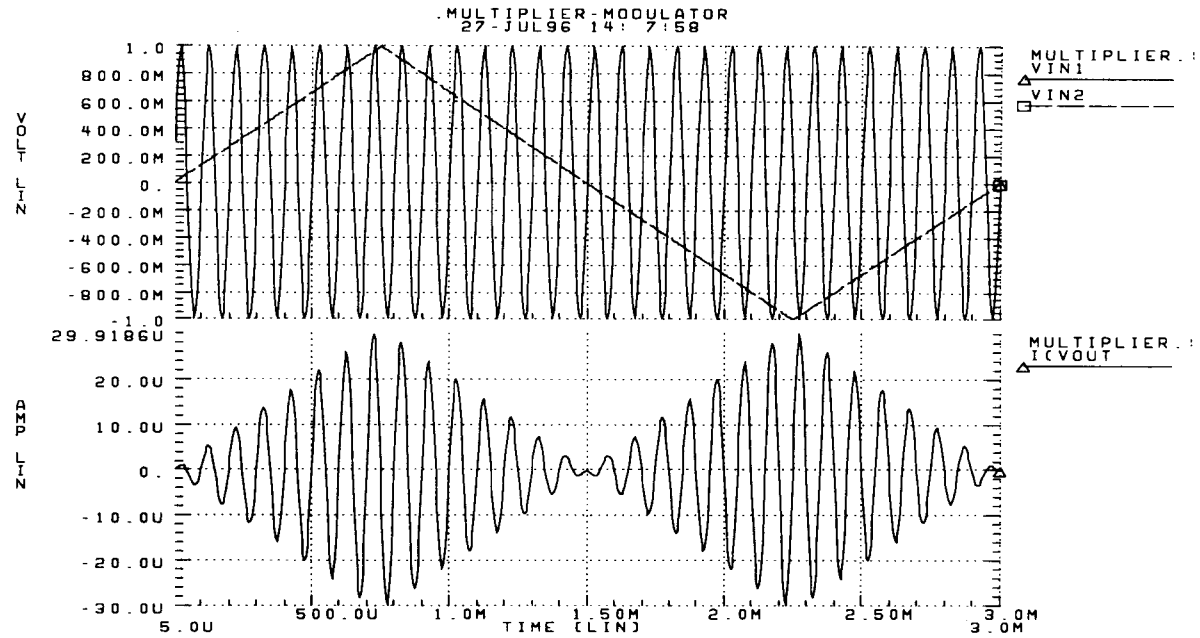
A chip containing a g_m–C fifth-order pulse-shaping filter having the normalized transfer function

$$H(s) = \frac{s(1513.6 - 76.52s + 38.45s^2)}{1681.8 + 1484.5s + 581.9s^2 + 128.6s^3 + 16.4s^4 + s^5}$$

was designed. Such a filter has a step response that is nearly triangular with its peak height occurring at some fixed delay after the step. This filter, with a delay tunable from 3–28 μs, was designed and fabricated using the MOSIS 2 μm orbit analog process. The filter was implemented as a cascade of g_m–C biquads [6]. Since the distortion specifications were not overly strict (<1% THD for $V_{\text{in}(p-p)} = 2$ V) and low complexity was desired, a single-ended filter configuration was used. The employed transconductance was the voltage-tunable one shown in Fig. 7(b). Fig. 9 shows the measured step responses of the filter for three different tuning voltages.



(a)



(b)

Fig. 13. (a) Simulated performance of the proposed multiplier. (a) As a frequency doubler and (b) as a modulator.

The main disadvantage of the voltage-tunable transconductor, in comparison with the current-tunable one, is that its intrinsic gain $(g_{m(\text{eff})} \cdot r_{\text{out}})$ varies as $g_{m(\text{eff})}$ varies, resulting in added loss to the transfer function that is dependent on the tuning. This tendency can clearly be seen in the Fig. 9 plot.

Fig. 10 shows the measured noise + distortion versus amplitude of the circuit's output for an input 30-kHz sine wave. The filter was tuned to give unity gain at this frequency. For amplitudes greater than 600 mV, the second-order harmonic dominates the distortion. This was not observed in simulations and, hence, is likely due to transistor mismatches since the transconductance block used in this filter is class AB and thus relies on symmetrical operation to cancel out even-order harmonics. Moreover, as the input frequency increases, the CMRR of the transconductance block's input differential pair decreases and the common-mode input voltage becomes signal dependent, thus increasing the amplitude of the second harmonic even further. This distortion could be reduced significantly by using careful layout techniques and fully differential topologies.

V. Differential Input Current Squaring Circuit and Four-Quadrant Quarter-Square Multiplier

The DAL can be used in several other (nonfiltering) applications. In Fig. 11 a differential input current squaring circuit

is shown. The following input–output relation can be derived using (5), (6), and the square-law voltage–current relation of a saturated MOS transistor:

$$I_{\text{out}} = 2\frac{\beta_2}{\beta_1}I + \beta_2 R^2 i_{\text{in}}^2. \tag{18}$$

A four-quadrant quarter-square voltage multiplier can easily be realized using two suitably driven Fig. 11 current squaring circuits. The full schematic of such a multiplier is shown in Fig. 12. Its operation is based on the realization of the following general relation:

$$AB = \tfrac{1}{4}[(A+B)^2 - (A-B)^2]. \tag{19}$$

The term "quarter-square," used to describe the multiplier, refers to the way the multiplication is performed—that is, a *quarter* of the difference of two *square* terms is taken. Hence to multiply the quantities A and B the following three operations must be performed. First, their sum $(A+B)$ and the difference $(A-B)$ (or signals proportional to them) must be generated. Then each of those signals must by squared and finally subtracted from each other. The circuit in Fig. 12 performs these three operations as follows.

1) The p-channel source-degenerated differential pairs M_{3A} and M_{3B} are used to convert the applied floating input voltages V_{in1} and V_{in2} into currents.

$$2i_{\text{in1}} = V_{\text{in1}}/R'_d \tag{20}$$
$$2i_{\text{in2}} = V_{\text{in2}}/R'_d \tag{21}$$

where $R'_d \equiv R_d + 1/g_{m3}$. The differential-pair input transistors are split into a pair of cross-coupled structures as shown in Fig. 12 so that the following two pairs of currents are created:

$$\begin{aligned}(I_1+I_2)+(i_{\text{in1}}+i_{\text{in2}}) &= (I_1+I_2)+\frac{1}{2R'_d}(V_{\text{in1}}+V_{\text{in2}})\\ (I_1+I_2)-(i_{\text{in1}}+i_{\text{in2}}) &= (I_1+I_2)-\frac{1}{2R'_d}(V_{\text{in1}}+V_{\text{in2}})\end{aligned} \tag{22}$$

and

$$\begin{aligned}(I_1+I_2)+(i_{\text{in1}}-i_{\text{in2}}) &= (I_1+I_2)+\frac{1}{2R'_d}(V_{\text{in1}}-V_{\text{in2}})\\ (I_1+I_2)-(i_{\text{in1}}-i_{\text{in2}}) &= (I_1+I_2)-\frac{1}{2R'_d}(V_{\text{in1}}-V_{\text{in2}}).\end{aligned} \tag{23}$$

2) By the use of two current squaring circuits in Fig. 11 the differential component of each pair is squared:

$$I_{\text{out}_1} = 2(I_1+I_2)+\frac{1}{4}\beta\left(\frac{R}{R'_d}\right)^2(V_{\text{in1}}+V_{\text{in2}})^2 \tag{24}$$

and

$$I_{\text{out}_2} = 2(I_1+I_2)+\frac{1}{4}\beta\left(\frac{R}{R'_d}\right)^2(V_{\text{in1}}-V_{\text{in2}})^2. \tag{25}$$

3) The two resulting currents I_{out_1} and I_{out_2} are finally subtracted at the output node:

$$i_{\text{out}} = \beta\left(\frac{R}{R'_d}\right)^2 V_{\text{in1}}V_{\text{in2}}. \tag{26}$$

This four-quadrant multiplier was simulated using BSIM models (level 13) for the MOSIS 2 μm orbit analog process . The tail currents of the differential-pair stages $(2I_1, 2I_2)$ were 50 μA. The degeneration resistors R_d were 20 k and the resistors used in the DAL were 5 k. The rest of the elements were as indicated on the schematic.

Fig. 13(a) shows the performance of the multiplier as a frequency doubler. The input signals are a pair of differential 1-kHz sine waves each having 1-V amplitude. Fig. 13(b) shows the multiplier performance as a modulator. A triangle wave with frequency 333 Hz and 1-V amplitude was applied to one of the inputs while a 10-kHz sine wave was applied to the other. The simulated bandwidth of the circuit is from dc to 10 MHz.

VI. Conclusion

A simple structure containing MOS transistors and resistors, which responds to a differential input current as a linear resistor while responding to the common-mode current as a diode-connected transistor, was presented. It is shown that these properties make it possible for the structure to directly drive a pair of MOS transistors realizing a tunable class-AB current gain and current squaring circuits. When driven by differential pair-based structures those two circuits can be used to build a block whose transconductance is proportional to the tail current and a four-quadrant voltage multiplier. Simulation and measured results for the above mentioned structures are included.

References

[1] G. J. Allbutt and D. G. Nairn, "Tunable capacitors for digital CMOS compatible high-frequency analog filters," in *Proc. Int. Symp. Circuits Syst.*, June 1996, pp. 89–92.
[2] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 357–365, June 1987.
[3] P. Hollis and J. Paulos, "Artificial neural networks using MOS analog multipliers," *IEEE J. Solid-State Circuits*, vol. 25, pp. 849–855, June 1990.
[4] F. Krummenacher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750–757, June 1988.
[5] J. Peña-Finol and J. Connelly, "A MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1064–1073, Dec. 1987.
[6] V. I. Prodanov and M. M. Green, "Biquad gm-C structures which use double-output transconductors," in *Proc. Midwestern Symp. Circuits Syst.*, Aug. 1995, pp. 170–173.
[7] E. Seevinck and R. Wassenar, "A versatile CMOS linear transconductor/square-law function circuit," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 366–377, June 1987.
[8] J. Silva-Martinez, M. Steyaert, and W. Sansen, "A large-signal very low-distortion transconductor for high-frequency continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 26, pp. 946–954, July 1991.
[9] C. Toumazou, F. J. Lidgey, and D. G. Haigh, *Analogue IC Design: The Current-Mode Approach.* London, England: Peregrinus, 1991, ch. 2.
[10] P. Van Peteghem, H. Fossati, G. Rice, and S. Lee, "Design of a very linear CMOS transconductance input stage for continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 25, pp. 497–501, Apr. 1990.

Vladimir I. Prodanov (S'96) was born in Sofia, Bulgaria, on February 3, 1970. He received the engineering degree (B.S.) from the Technical University, Sofia, Bulgaria, in 1991 and the M.S. degree in electrical engineering in 1994 from the State University of New York, Stony Brook, where he is currently working toward the Ph.D. degree.

His research interests include analog (continuous-time) integrated circuits with low supply voltage emphasis.

Michael M. Green (S'88–M'92) received the B.S. degree in electrical engineering from University of California, Berkeley, in 1984 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, in 1988 and 1991, respectively.

From 1984 to 1987 he was a design engineer in National Semiconductor's audio integrated circuit design group. He is currently an Associate Professor of electrical engineering with the University of California, Irvine. His research interests include nonlinear circuit theory, analog integrated circuit design, and analog circuit simulation.

Dr. Green is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi. From 1992 to 1994 he was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS — I and of the IEEE TRANSACTIONS ON EDUCATION, and was Chair of the CAS Nonlinear Circuits and Systems Technical Committee. He was the recipient of the Outstanding Master's Degree Candidate Award in 1989 and the Outstanding Ph.D. Degree Candidate Award in 1991, both from the UCLA School of Engineering and Applied Science. He is also the recipient of the Sigma Xi Prize for Outstanding Graduate Science Student at UCLA in 1991, the 1994 Guillemin-Cauer Award of the IEEE Circuits and Systems Society, the 1994 W. R. G. Baker Award of the IEEE, the 1996 IEEE Region 1 Award for Technical Excellence, and a 1994 National Young Investigator Award from the National Science Foundation.