CMOS current mirrors with reduced input and output voltage requirements

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A CMOS current mirror with lower than V\text{sub} input voltage requirement is presented. It is shown that the structure can be modified to provide cascode-type output resistance for output voltages even lower than 2V\text{sub}. The topology of the proposed current mirror allows low distortion operation from a single 1.5V supply, which makes it attractive for low-voltage applications.

Introduction: The current mirror is one of the most important building blocks of analogue integrated circuits. Modern VLSI systems now operating from single 3.3V supplies and dropping, require high performance current mirrors that can operate with low voltages. The fact that the V\text{sub} mirrors reported in the literature does depend on the threshold signal swing [1]. These topologies are commonly referred to as 'high-swing cascades'. However, the input voltage of most current mirrors reported in the literature does depend on the threshold voltage V\text{th}. This voltage drop (visually in the order of a volt) across the input terminal of those current mirrors may not be tolerable in all low-voltage applications. The use of current mirrors with low input voltage is especially important for implementation of VLSI test circuits which employ current sensing techniques [4].

Recently a few different current-mirror topologies with reduced input voltage requirements have been reported [4-6]. The topology capable of providing both low distortion and high bandwidth while having no hard dynamic range limitation is shown in Fig. 1 [4]. The level-shifter \( V_b \) in Fig. 1a can be implemented as shown in Fig. 1b. In this case, its value is equal to the difference of \( V_{ds} \) and \( V\text{sub} \), and can be set by properly selecting the aspect ratios and the values of current sources \( I_n \) and \( I_m \). In general, it is assumed that for linear operation, both transistors forming the current mirror (\( M_{m1}, M_{m2} \)) must be kept in saturation. Hence, the required \( V_b \) must be smaller than the threshold voltage \( V\text{th} \).

In this Letter we show that even if \( M_{m1} \) is biased in the triode region the Fig. 1a configuration will perform linear current mirroring. As a result, two new current-mirror circuits with reduced input, output and supply voltage requirements are derived.

**Low input-voltage current mirrors using triode-region transistors:**

For the Fig. 1a circuit, assume that \( V_b \) is given by

\[
V_b = V_{ds} + \Delta V
\]

where \( \Delta V \geq 0 \). Under this condition transistor \( M_{m1} \) is biased in triode and its drain current \( I_{m1} \) in first approximation is given by

\[
I_{m1} = \frac{\beta M_{m1} (V_{gs} - V_{th}) V_{ds}}{2} = \frac{\beta M_{m1} V_{ds}}{2}
\]

Using eqns. 1 and 2 and the Fig. 1a schematic diagram the input current \( I_n \) can be expressed as

\[
I_n = I_{m1} = \frac{\beta M_{m1}}{2} (V_{gs} - V_{th})^2 = \frac{\beta M_{m1}}{2} (\Delta V)^2
\]

The last equation shows that a triode-region transistor conducting drain current \( I_n \) and having a voltage source with the value \( V_{bs} + \Delta V \) connected between its gate and drain terminals, has the same gate potential as that of a transistor in saturation conducting current \( I_n + \beta M_{m1} V_{ds} \). Since \( M_{m1} \) is still assumed to be in saturation the output current of the Fig. 1a current mirror must be given by

\[
I_{out} = I_n + \frac{\beta M_{m1}}{2} V_{ds}^2
\]

where \( \beta M_{m1} = \beta_0 \).

**Fig. 2 Implementation of required level-shifter**

a) Simple current mirror using triode-region transistor

b) Triode-region current mirror with cascode-type output resistance

There are numerous possibilities for the level-shifter realisation. The level-shifter employed in the Fig. 1b circuit may be used providing the difference between the gate potentials of \( M_{m1} \) and \( M_{m2} \) satisfies eqn. 1, but the minimal supply voltage required in this case must be higher than \( V_{ds} + V_{th} \). Another simpler and more robust implementation of the required level-shifter is used in the Fig. 2a current mirror. It consists of a single diode-connected n-channel transistor \( M_n \) conducting some constant bias current \( I_n \).

The \( V_b \) of this circuit is thus given by

\[
V_b = V_{GS} = V_{in} + \sqrt{\frac{2}{\beta_0}} I_n
\]

The output current of this structure can be found to be

\[
I_{out} = I_{in} + \left( 1 + \frac{\beta M_{m1}}{\beta_0} \right) I_n
\]

It must be noted that the Fig. 2a mirror requires lower supply voltages than the Fig. 1b mirror. For threshold voltages \( V_{th} = 0.9 \) V the required \( V_{ds} \) is in the order of 1.3 - 1.5V. The main disadvantage of the proposed mirror is that its output current has an offset term.

**Fig. 3 Input and output characteristics of circuit in Fig. 2b**

a) Input driving-point characteristic \( V_{in} \) against \( I_{in} \) of Fig. 26 circuit

b) Output characteristic \( I_{out} \) against \( V_{out} \) for \( I_{in} = 50 \mu A \)

c) \( I_{out} \) against \( V_{gs} \) for \( I_{in} = 50 \mu A \)

A structure which possesses a cascode-type output resistance, has better symmetry and cancels the current offset term is shown in Fig. 2b. Here negative feedback is formed by \( M_{m1}-M_{m2}, M_{m1}-M_{m2} \) and \( M_{m2} \) and the output resistance is approximately given by

\[
r_{out} = \frac{\beta_0}{\beta_0 + \beta M_{m2}} r_m \text{f}_{m1}(r_{m1} | V_{in})
\]
Simulation results: Both circuits shown in Fig. 2 were simulated using a BSM level-13 model provided for MOSIS 2 micron analog process. The total harmonic distortion of the Fig. 2a and b mirrors was better than 0.3 and 0.1%, for input with amplitude 75μA and frequency 1kHz and $I_1 = 10μA$, respectively. This distortion can be accounted for if a more precise model for transistors in the triode region is to be used. The simulated input and output characteristics and $I_{out}$ against $V_{ds}$ for $I_s = 50μA$ of the Fig. 2b circuit are shown in Fig. 3. Fig. 4 shows its simulated transfer characteristic and magnitude frequency response. The transistor sizes used were: $M_{102}$, and $M_{12}$ = 100/2, $M_{22}$ = 2004 and $M$ = 2002. In all simulations a single 1.5V supply was used. The simulated output resistance of the Fig. 2b was 1 MΩ for output voltages as low as 250mV.

Conclusion: MOS current mirrors with reduced input and output voltage requirements are derived. They used suitably biased triode-region transistors and have no hard limit on their dynamic range.

References


Precision temperature stabilised tunable CMOS current-mirror for filter applications

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A temperature stable external reference resistor is used to accurately control and tune the transconductance of an integrated current-mirror. The technique can be used to tune and optimize the bandwidth of the current-mirror for application in CMOS filters.

Introduction: Current-mode continuous-time filters which exploit a generic CMOS current-mirror are very promising for high frequency applications, and have lately been investigated considerably [1]. In this Letter we present a temperature stable resistive tuning compensation scheme to accurately adjusting the bandwidth of the current-mirror and hence the filter operating frequency.

Basic current mirror: As discussed in [2], the bandwidth of the simple CM can be increased with resistive compensation as shown in Fig. 1a. All the CMs in this Letter are assumed to be appropriately biased, so biasing circuits are not shown. For $R_c = 1/2g_{m1}$ the resultant bandwidth is doubled (assuming $M_1$ and $M_2$ are the same size). This technique is also applicable to first generation switched-current cells and other more complicated CMs such as cascode, regulated cascode and the Wilson CM.

For full monolithic integration, $R_c$ can be a passive resistor made of polysilicon, or a diffusion resistor. There are three disadvantages of using such passive resistors in this application. First, the absolute values of the integrated passive resistors have a rather large tolerance. Even with a mature process, the passive and active components can have more than 10% variations. Secondly, the temperature dependence of passive resistors does not track transconductance of the MOS transistors. Third, for optimum compensation, it is required that $R_c = 1/2g_{m1}$. Hence, $R_c$ is required to track $g_{m1}$ which varies considerably with process and temperature drifts. For more robust design, $R_c$ can be replaced by a small transistor $M_3$ with its gate voltage $V_{g3}$ tunable. This will incur little extra power consumption and minimal increase in chip area.

Active $R_c$ tuning: First, we analyze the resistive compensation. Referring to Fig. 2, $M_{11}$, $M_{12}$, and $M_{22}$ produce $g_{m1}$, which controls the gate voltage of $M_{10}$. The channel resistance of $M_{10}$ needs to match $g_{m1}$ and to track $1/g_{m1}$ for optimum bandwidth [3]. With $(W/L)_{1} = (W/L)_{2}, M_{10}$ and $M_{22}$ are biased with the same current, $I_c$. Further, if $(W/L) = (W/L)_{1}$, the voltage at node 1 will be the same as at node 2. With the gate of $M_{12}$ and $M_{22}$ at equal potential $V_{gs3} = V_{gs2}$. To keep the voltage at node 1 and node 2 the same, the tuning current, $I_{tune}$, which feeds into the drain of $M_{12}$ must be drawn out from its source to maintain $I_{tune} = I_{tune}$ (this can be implemented with a simple sink/source CM). With these conditions, and assuming $M_{10}$ is operating in its linear region, and $M_{10}$, $M_{12}$, and $M_{22}$ are biased in saturation, the following equations are derived

$$g_{m1} = \sqrt{2\mu C_{ox}(W/L)_{1}I_{1}}$$

$$r_{ds3} = \frac{1}{\mu C_{ox}(W/L)(V_{gs3} - V_{t})}$$

$$I_1 + I_{tune} = 0.5g_{m1}(V_{gs3} - V_{t})^2$$

where all the symbols have their usual meanings [3], Eqsns. 1 - 3 are combined in eqn. 4 to give a better insight to the tuning and control mechanism.

$$I_{tune} = \left[ \frac{1}{2\mu C_{ox}(W/L)_{1}V_{gs3} - 1} \right] I_1$$

Note that for $I_1 = 0$, an optimum transistor size relationship exists which is only dependent on the transistor aspect ratios and it is well controlled.