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Bipolar/CMOS (weak inversion) rail-to-rail constant-g_m input stage

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Indexing terms: Bipolar integrated circuits, CMOS integrated circuits

A rail-to-rail constant-g_m input stage suitable for bipolar or weak inversion CMOS implementation is presented. To achieve rail-to-rail operation, two complementary differential pairs driven in parallel are used. To guarantee constant net transconductance each differential pair is augmented with a suitable biasing circuit. The biasing circuits are implemented without current mirrors, which results in low sensitivity to process variations and potentially higher bandwidth.

Introduction: A common way to achieve a rail-to-rail input range when designing low-voltage op-amps is to connect *n*-type (i.e. either *npn* or *n*-channel) and *p*-type differential pairs in parallel and sum their small-signal currents. In the Fig. 1*a* circuit, the required summation is performed in the gain stage. Performing this guarantees that for any common-mode input voltage at least one of the differential pairs will operate properly as long as $V_{DD} > 2V_t + 4\Delta V_{GS}$.

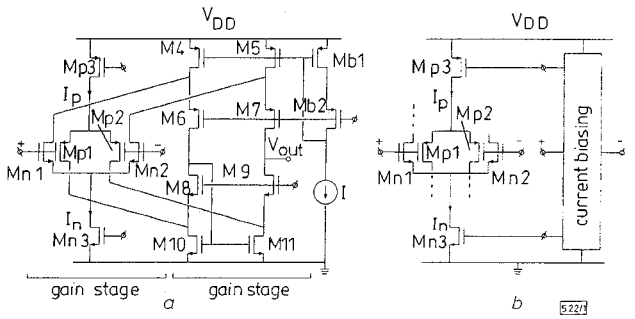

Fig. 1 *Op-amp with simple rail-to-rail input stage and conceptual schematic of rail-to-rail input stage having common-mode dependent current biasing*

a Op-amp with simple rail-to-rail input stage
b Conceptual schematic diagram of rail-to-rail input stage

The main disadvantage of this simple rail-to-rail input stage is the fact that its net transconductance g_{m_T} varies by a factor of 2 over the common-mode range. In the mid-supply range, where both pairs operate with their nominal currents, this transconductance is given by

$$g_{m_T} = g_{m_n} + g_{m_p} \quad (1)$$

where g_{m_n} and g_{m_p} are the transconductances of the NMOS and PMOS differential pairs, respectively. As $V_{in_{CM}}$ approaches the negative (positive) rail, I_n (I_p) becomes 0 and g_{m_T} reduces to g_{m_p} (g_{m_n}). This variation makes it impossible to optimally frequency compensate an op-amp using such an input stage. In addition, it may cause increased distortion levels.

To reduce the variation of the net transconductance, the use of common-mode dependent current biasing has been proposed. The idea is to balance out the change in g_{m_n} and g_{m_p} by suitably controlling the tail currents I_n and I_p (e.g. Fig. 1*b*). Since the transconductance of both bipolar and weak inversion CMOS differential pairs is proportional to the tail current, to keep g_{m_T} constant the following condition must be satisfied:

$$I_n + I_p = constant \quad (2)$$

A few circuits realising this relation have been proposed [1–4]. Most of them, however, use one or more current mirrors [1–3]. The use of current mirrors is undesirable for at least two reasons. First, any current mirror mismatch directly translates into a proportional variation of net transconductance. This could prove disastrous in the CMOS case because the accuracy of a current mirror operating in weak inversion is generally quite poor. Secondly, every current mirror introduces a pole with magnitude $g_m/2C_\pi$ ($g_m/2C_{gs}$) for the bipolar and MOS case respectively; hence the use of current mirrors limits the bandwidth of the current biasing circuit.

In this Letter we derive a new topology which does not use current mirrors. In addition, unlike the structure reported in [4] it has no nodes which exhibit high voltage excursions in response to common-mode input voltage. As a result, higher bandwidth and improved robustness to processing variations can be expected.

Proposed topology: Instead of trying to directly realise the constraint given in eqn. 2 we take the alternative approach of modifying each differential pair separately in such a way that they become fully complementary. In the context of this discussion, the above term refers to the situation in which the transconductances of two independent input stages vary with the input common-mode voltage but their sum stays constant over the entire common mode range.

In this Section, a weak inversion CMOS input stage will be derived. However, any comment made or conclusion drawn about the operation of this circuit will be valid for its bipolar counterpart as well.

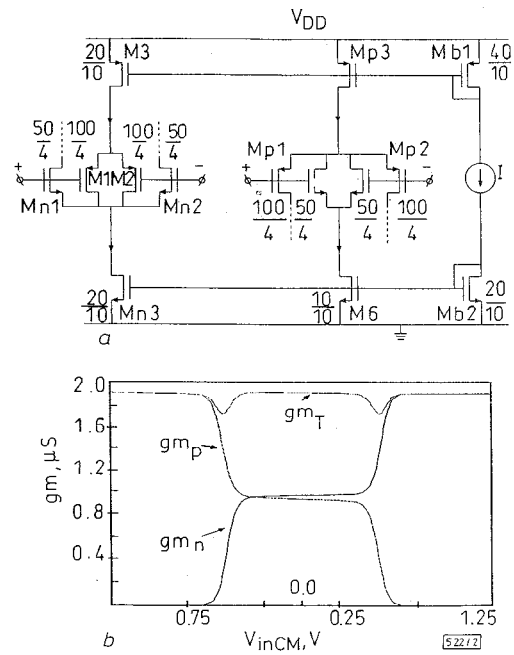

Fig. 2 *Rail-to-rail input stage using two 3-region stages*

a Schematic diagram
b Results of HSPICE simulation illustrating variation of individual and net transconductances against $V_{in_{CM}}$

The first step towards full complementarity is to make sure that within the three well defined regions of operation (near-ground, mid-supply and near-V_{DD}), the net transconductance g_{m_T}, has the same value. To do this we need to modify the M_{n1-n3} (M_{p1-p3}) differential pair so that its transconductance is 0 (g_m) for $V_{in_{CM}}$ near ground, $g_m/2$ for $V_{in_{CM}}$ near mid-supply, and $g_m(0)$ for $V_{in_{CM}}$ near V_{DD}. This task is readily accomplished without the use of current mirrors by connecting two additional differential pairs, M_{1-3} and M_{4-6}, as shown in Fig. 2*a*. The tail currents of these pairs have a nominal value of half that of the M_{n1-n3} and M_{p1-p3} differential pairs.

If transistors M_{1-3} (M_{4-6}) and M_{p1-p3} (M_{n1-n3}) were perfectly matched and the currents they conduct were the same, the sum $g_{m_n}+g_{m_p}$ would be constant not only in the near-rail and mid-supply regions but also in the transition regions. Unfortunately, the Fig. 2*a* circuit does not meet these requirements. The reason is that transistors M_3 (M_6) and M_{p3} (M_{n3}) differ in both aspect ratios and operation. Transistor M_3 (M_6) provides the tail current of $M_{1,2}$ ($M_{4,5}$) differential pair, while transistor M_{p3} (M_{n3}), in addition to providing the tail current of $M_{p1,p2}$ ($M_{n1,n2}$) differential pair, sinks the current conducted by M_6 (M_3). Because of these differences, when $V_{in_{CM}}$ approaches the positive (negative) rail transistors M_3 (M_6) and M_{p3} (M_{n3}) do not enter the triode region simultaneously. As a result the $0 \rightarrow g_m/2$ and $g_m/2 \rightarrow g_m$ transitions of the M_{n1-n3}/M_{1-3} stage do not coincide with $g_m \rightarrow g_m/2$ and $g_m/2 \rightarrow 0$ transitions of the M_{p1-p3}/M_{4-6} stage. This causes 'glitches' with magnitude 10–15% of the nominal value of g_{m_T} to occur in the net transconductance (e.g., Fig. 2*b*). For some applications, this variation could be acceptable; however, in general we would prefer to have g_{m_T} as flat as possible.

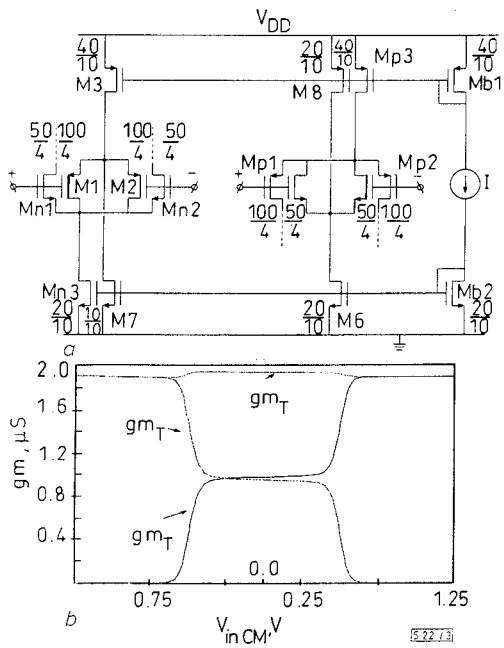

Fig. 3 *Rail-to-rail input stage using two fully complementary stages*

a Schematic diagram
b Results of HSPICE simulation illustrating variation of individual and net transconductances against $V_{in_{CM}}$

To do this we increase the nominal value of the currents conducted by M_3 and M_6 to I and sink the 'unwanted' $I/2$ portion through additional current sources realised in Fig. 3*a* by transistors M_7 and M_8. By doing this, transistors M_3 and M_6 are forced to behave in an identical way to that of transistors M_{p3} and M_{n3}, respectively. The last modification makes the two structures $M_{n1-n3}/M_{1-3}/M_7$ and $M_{p1-p3}/M_{4-6}/M_8$ fully complementary and as expected, eliminates the g_{m_T} variation in the transition regions, as shown in Fig. 3*b*.

Notice that the only transistors connected in a current mirror configuration are those providing the constant current biasing. Since these transistors have little influence on the speed of the developed current biasing circuit and are generally not required to be in weak inversion, they can be sized such that the mismatch between their drain currents is as small as possible.

Simulation and experimental results: The data in Figs. 2*b* and 3*b* come from an HSPICE simulation of the corresponding weak inversion CMOS circuits using BSIM (level 13) models provided by MOSIS for the 2μm ORBIT analogue process. A supply voltage of 2.5V and nominal bias current I of 100nA were used. The transistor aspect ratios were as given on the schematic diagrams. The 2% deviation of g_{m_T} in Fig. 3*b* can be attributed to second-order effects, such as variation of the slope factors of weak inversion transistors with the source-bulk voltage and finite output resistance.

Qualitatively similar results were obtained from equivalent bipolar circuits which were realised using discrete National Semiconductor MPQ3904 and MPQ3907 components.

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Double-edge-triggered address pointer for low-power high-speed FIFO memories

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Indexing terms: Integrated memory circuits, VLSI

The clock line, which is used to shift the addresses in the address pointer circuit of an FIFO, has a large load capacitance and hence large power consumption is required to drive the line. Furthermore, the large load capacitance limits the speed of operation of the FIFO. The authors develop a double-edge-triggered technique for address pointer design. By using the proposed technique, the high-speed FIFO operation can be realised with relatively lower shift clock frequency. The power consumption of the new circuit is significantly reduced due to the reduction of the shifting clock frequency as well as the cumulative load capacitance on shifting clock lines.

Introduction: In FIFO memories, data that are written into the RAM's storage area are read out in the same order. The FIFO operations are controlled by special address pointers that keep track of where data are to be written and from where they are to be read. The function of such address pointers is normally implemented by shift register chains. During operations, a high level signal is transferred along the register chain and the high state of a register results in the corresponding row select line and column select line being activated. Therefore, the memory cells can be accessed by a specific sequence by the control of the shift clock signal. To guarantee that data are only shifted to the next stage register during one shift clock cycle, the shift register chain is usually constructed by a master-slave D flip-flop which consists of two D latches. Traditionally, the implementation of the D latch can be based on either a CMOS transmission gate or tri-state buffer as described in [1, 2]. However, both kinds of D latches contribute relative large load capacitance to shift clock lines. The cumulative large load capacitance on shifting clock lines limits the speed of performance, and also causes large power consumption