ANALYSIS & DESIGN OF IMPROVED MULTIPHASE INTERLEAVING DC-DC CONVERTER WITH INPUT-OUTPUT BYPASS CAPACITOR

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ABSTRACT

ANALYSIS & DESIGN OF IMPROVED MULTIPHASE INTERLEAVING DC-DC CONVERTER WITH INPUT-OUTPUT BYPASS CAPACITOR

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As the transistor count per chip in computer microprocessors surpasses one billion, the semiconductor industry has become more and more concerned with meeting processor’s power requirements. This poses a design challenge for the power supply module, especially when the processor operates at low voltage range. For example, the electrical requirement for the newest Intel microprocessors has exceeded 100A with an input voltage of approximately 1V. To overcome this problem, multiphase DC-to-DC converters encased in a voltage regulator module (VRM) have become the standard means of supplying power to computer microprocessor.

This study proposes a new topology for the multiphase DC-to-DC converter for powering microprocessors. The new topology accepts 12 V input, and outputs a steady state voltage of 1 V with a maximum output current of 40 A. The proposed topology aims to improve the input and output characteristics of the basic multiphase “buck” converter, along with an improved efficiency, line regulation, and load regulation.

To explore the feasibility of such a topology, open-loop computer simulation and closed-loop hardware tests were performed. On open-loop simulation, OrCad pspice was used to verify design calculations and evaluate its performance. Then the closed-loop hardware prototype was tested to compare the circuit performance with those values obtained from simulation.

The result shows the proposed topology improvement of efficiency, board size, output ripple, and regulations.
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INTRODUCTION

As microprocessor transistor density increases following Moore’s Law, concern grows in the semiconductor industry over powering CPUs reliably and efficiently. Moore’s Law, surmised by Intel’s co-founder Gordon Moore in 1965, predicts that the number of transistors in a single processor will double approximately every two years (“Moore’s Law.” par. 4). Intel’s latest Dual Core Itanium 2 processor has over one billion transistors. Powering these processors requires a special kind of power supply capable of producing high current output at low voltages. Computer power supplies must keep evolving to meet the future demands of microprocessors.

The typical computer power rail of the system board provides 12 V (Intel VRM 8). The rail voltage needs to be converted to the specified processor voltage without incurring a large power loss within the converter circuitry; therefore, more efficient multi-phase DC-to-DC converters have become the norm for powering microprocessors. The higher frequency is needed due to heat consideration when powering microprocessor. However, as processor voltage ratings decrease and current ratings increase, the challenge to produce a converter that will supply the power without sacrificing efficiency and output quality, becomes more difficult.

The intention of this project is to introduce and analyze a new multi-phase DC-to-DC converter topology aimed at improving the delivery of power to a microprocessor. If successful, the topology will improve the output voltage and current characteristics such as peak to peak ripple and regulations while improving overall converter efficiency.

1.1 Overview of Power Electronics

Power electronic devices convert one type of electrical power to another, reduce or increase voltage and current, or help compensate for power system deficiencies. As a field of study, power electronics
blends three electrical engineering disciplines: power, electronics, and control [1]. The field continues to evolve, producing innovative and cutting edge technology to manage the power demands of our modern society. High voltage power electronic applications include converting high voltage AC power (e.g. megawatts) to HVDC for transmission, compensating transmission lines, or controlling power flow. Low voltage applications include DC motor drives, DC power supplies, and low voltage rectifiers.

The DC to DC conversion also involves a voltage level change from one to another. This converter, also known as a “chopper” or “switching regulator,” controls its average output voltage by varying the time that its input transistor is closed. The converter is being used heavily in Switch Mode Power Supply (SMPS). Depending on the topology, a DC to DC converter can be used to step-up (Boost) a voltage, step-down (Buck) a voltage, or even both (Buck-Boost). We will deal mainly with the Buck Converter since it is the heart of the Multiphase topology conducted in this thesis. The “buck” converter is the most common configuration for microprocessor power applications because the output voltage is always from the input to be reduced.

1.2 The Buck Converter

A common DC-to-DC converter is the buck converter or buck regulator as shown in Figure 1.1. The main function is to reduce or “buck” its average input voltage to a lower average output voltage. A buck converter consists of three main parts which are switch, diode, and inductor. An inductor is being used as an energy storage element while the switch acts as a gate for energy flow, and the diode...
allows energy to freewheel when needed. The switch is controlled by an external controller that closes (turns on) the switch for a certain percentage of the switching period. This percentage is known as the duty cycle, $D$, of the switch and is defined as the on-time, $t_{on}$, of the switch divided by the switching period $T$, and is given by the expression:

$$ D = \frac{t_{on}}{T} \quad (1-1) $$

The inductor $L$ acts as an energy storage element and supports the load when the switch is off. Hence, it is an important consideration when choosing a value for the inductor.

When the switch is closed at $t = 0$, the inductor charges and current through it increases to a maximum value after the time duration $t_{on}$. Assuming ideal circuit elements with constant input voltage $V_{in}$ and output voltage $V_{out}$, the voltage across the inductor $v_L$ during this time is given by:

$$ v_L = V_{in} - V_{out} = L \frac{di_L}{dt} \quad (1-2) $$

Rearranging the equation yields a positive linear slope for inductor current while the switch is closed:

$$ \frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} = \frac{\Delta i_L}{t_{on}} \quad (1-1) $$

Solving equation (1.1) for $t_{on}$, substituting into equation (1.3), and solving for $\Delta i_L$ produces an expression for the change in inductor current when the switch is closed:

$$ \Delta i_L = \frac{V_{in} - V_{out}}{L} DT \quad (1-2) $$

After reaching $t_{on}$ the switch opens and the inductor current “freewheels” through the load and the diode, decreasing during the time duration $t_{off}$ to a minimum value at the end of the switching period. After following the same procedure that produced equations 1.2-1.4, the change in inductor current with the switch in an open state can be expressed as:

$$ \Delta i_L = -\frac{V_{out}}{L} (1 - D) T \quad (1-3) $$
The change in inductor current $\Delta I_L$ represents the peak-to-peak ripple current of the inductor.

A buck converter can enter two distinct operation modes: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). The value of the inductor determines whether the converter runs in CCM or DCM per given minimum output load and switching frequency.

### 1.2.1 Continuous Conduction Mode

Referring to Figure 1-1, in Continuous Conduction Mode, current will flow from input thus charging the inductor when the switch is closed and the diode is reverse biased. In steady state condition, the voltage across the inductor when the switch is closed is

$$ V_{L_{sw\_Closed}} = (V_{IN} - V_{OUT}) $$

When the switch is opened and the diode is forward biased, the voltage across the inductor would be equal to

$$ V_{L_{sw\_Open}} = -V_{OUT} $$

Since an average inductor voltage at steady state is equal to zero based on the Voltage-Second Balance concept; then we can derive a transfer function for buck converter:

$$ V_{L_{sw\_Closed}} * t_{ON} + V_{L_{sw\_Open}} * t_{OFF} = 0 $$

$$ V_{L_{sw\_Closed}} * DT_{SW} + V_{L_{sw\_Open}} * (1 - D)T_{SW} = 0 $$

$$ (V_{IN} - V_{OUT})* DT_{SW} - V_{OUT} * (1 - D)T_{SW} = 0 $$

$$ (V_{IN} - V_{OUT})* DT_{SW} = V_{OUT} * (1 - D)T_{SW} $$

$$ V_{IN} * D = V_{OUT} $$
From equation above, it can be seen that the average output voltage of a buck converter is controlled by the duty cycle factor and its value is always less than input voltage.

Throughout the switching period, inductor is being charged and discharged by the switching action. Inductor current ramps up with a positive slope when the switch is on and ramps down with a negative slope when the switch is off. Its ripple value can be calculated using the following equation.

When switch is on:

\[
V_{L,\text{sw}_{\text{on}}} = L \frac{di_L}{dt}
\]

\[
\frac{di_L}{dt} = \frac{V_{L,\text{sw}_{\text{on}}}}{L}
\]

\[
\Delta i_L = \frac{(V_{IN} - V_{OUT})}{L}
\]

\[
\Delta i_L = \frac{(V_{IN} - V_{OUT})}{L} \Delta T_{SW}
\]  

(1-6)

Since \(V_{IN}\) is always greater than \(V_{OUT}\) then we can verify that the slope for inductor current will always be positive when the switch is on.

When switch is off:

\[
V_{L,\text{sw}_{\text{off}}} = L \frac{di_L}{dt}
\]

\[
\frac{di_L}{dt} = \frac{V_{L,\text{sw}_{\text{off}}}}{L}
\]

\[
\Delta i_L = \frac{-V_{OUT}}{L}
\]

\[
\Delta i_L = \frac{-V_{OUT}}{L} \Delta T_{SW}
\]  

(1-7)

The negative sign Equation (1-7) shows that the inductor current ramps down when the switch is off based on equation above.
Again, referring to Figure 1-1, we can see the average inductor current value will be equal to the average output current because the average value for capacitor current will be zero. Based on equation (1-6) and (1-7) the maximum and minimum inductor current value will be equal to

\[
I_{L_{\text{max}}} = I_{L_{\text{avg}}} + \frac{\Delta i_L}{2}
\]  
(1-8)

\[
I_{L_{\text{min}}} = I_{L_{\text{avg}}} - \frac{\Delta i_L}{2}
\]  
(1-9)

We can use either value for \(\Delta i_L\) because the magnitude of \(\Delta i_L\) will be the same when the switch is on or off in the steady state. The only difference would be a negative sign when the switch is off.

In order to maintain CCM mode, inductor current should not reach zero when the switch is off. A critical value for CCM mode happens when the inductor current value is exactly equal to zero. Therefore, based on information above, the minimum inductance value can be calculated using equation (1-9)

\[
I_{L_{\text{min}}} = I_{L_{\text{avg}}} - \frac{\Delta i_L}{2}
\]

Setting \(I_{L_{\text{min}}} = 0\) to obtain the minimum inductance yields:

\[
0 = I_{L_{\text{avg}}} - \frac{\Delta i_L}{2}
\]

\[
0 = I_{OUT} - \frac{V_{OUT}(1-D)}{2Lf_{SW}}
\]

Rearranging:

\[
I_{OUT} = \frac{V_{OUT}(1-D)}{2Lf_{SW}}
\]  
(1-10)

Solving for L, and noting that the inductance value is the minimum inductance value \(L_{\text{min}}\) for CCM to occur:
Another component that is critical on a buck converter is the output capacitor. This capacitor keeps the output voltage ripple into a tolerable amount. Its value can be found using [1]:

\[
C_{OUT} = \frac{(1 - D)(V_{OUT})}{8Lf^2} \left( \frac{V_{OUT}}{\Delta V_{OUT}} \right)
\]  \hspace{1cm} (1-12)

1.2.2 Discontinuous Conduction Mode

This mode occurs when the inductance of buck converter is chosen to be below its critical value per given switching frequency and minimum load. Low value of inductance causes a large peak to peak ripple on inductor current. This in turn causes the converter to operate on discontinuous conduction mode at low load condition.

When the converter operates at this mode, the transfer function will be different from CCM mode buck. It can be proven that new expression for the average output voltage would be given as:

\[
V_{OUT} = V_{IN} \left[ \frac{2D}{-D + \sqrt{D^2 + \frac{8L}{RT_{SW}}}} \right]
\]  \hspace{1cm} (1-13)

From equation above, the average output voltage no longer depends solely on duty cycle; but instead it’s a function of inductance, output resistance and switching period. A buck converter operating in this mode is not preferred because of the complexity that is involved in designing a DCM buck converter.
The synchronous buck converter uses a semiconductor switch in place of the diode as illustrated in Figure 1-2, found on the asynchronous buck converter. Therefore there are two MOSFET in a single buck converter. The MOSFETs are called the high-side MOSFET and low-side MOSFET. These two MOSFETs do not turn on at the same time. If they do, then the input will be shorted to ground. In order to prevent this from happening, usually a MOSFET driver has a shoot through protection built in. The driver would create enough dead time between the two MOSFET such that the switching signals do not overlap each other. The switch, activated by the same control circuit that activates the input switch, allows an improved path for inductor current when the input switch is open. Compared to a diode, the switch provides a lower voltage drop, which improves overall converter efficiency by reducing power loss during conduction.

The main purpose of synchronous buck is to increase efficiency. MOSFETs are known to have a much lower voltage drop compared to Schottky rectifying diodes. These characteristics make MOSFETs more favorable than standard Schottky diodes for high current applications.
Chapter 2. Voltage Regulator Module & Multiphase Buck

2.1 What is Voltage Regulator Module?

According to [5] “A voltage regulator module (VRM) is an installable module that senses a computer’s microprocessor voltage requirements and ensures that the correct voltage is maintained’.

As microprocessor transistor’s density increases following Moore’s Law, concern grows in the semiconductor industry over powering CPUs reliably and efficiently. Moore’s law, surmised by Intel’s co-founder Gordon Moore in 1965, predicts that the number of transistors in a single processor will double approximately every two years. Powering these processors requires a special kind of power supply capable of producing high current output at low voltages. However, technical conflicts arise when the power supply to these microprocessors, widely known as Voltage Regulator Module (VRM), is operated at voltage below 1V as discussed in later section. The challenge will even be more since in 2010 microprocessors are expected to draw 150 A with 0.8 V supply voltage.

![Figure 2-1 Moore's Law [2]](image-url)
A voltage regulator module (VRM) is a special DC-DC converter that provides the necessary power into a microprocessor. This converter can be either soldered on to the motherboard or it could be provided by a module attached to the board. Typically, VRMs employ Buck converters in parallel to achieve the low output voltage at high output power. The goal of using VRM is to achieve a low cost power supply with high efficiency and high power density. Power density is defined as the volume in which the converter is housed. VRMs must be designed to provide tight tolerance at its output voltage due to the sensitivity of microprocessors. If the output voltage was to fall too low, then the microprocessor would turn off. On the other hand, if the output voltage is too high, then the microprocessor could be destroyed.

2.2 Disadvantages & Challenges of VRM

One of the challenges for VRM implementing buck converter would be a very small duty cycle, since the output voltage is decreased to a level significantly lower than the input voltage. A VRM with an input of 12 V and an output of 1 V yields a theoretical duty cycle of \( \frac{1}{12} = 8.3\% \).

There are some disadvantages in having a low duty cycle in a dc-dc converter.

1. This causes higher switching losses, which equate to lower efficiency [2]. When switching frequency is increased, then more switching loss will occur at the top MOSFET as well as an increase in MOSFET’s gate drive and body diode losses. This is due to the output capacitance of the Top MOSFETs being charged while idling. Consequently, efficiency will drop to less than 80% when switching frequency is increased into multi-MHz.

2. Low duty cycle causes a drop in the transient response. A slow transient response can destroy the microprocessor or cause undesirable performance from the microprocessor if the output voltage was to fall to high. This translates to switch loss proportional to \( \frac{1}{2}CV^2f \). [3].
3. It causes the 12 V to directly supply energy to the microprocessor for a shorter period of time. This implies the need of larger output capacitors to provide ample energy support. This in turn means that the VRM would be more costly, have a lower power density, and have a lower efficiency, due to the increase size of the capacitors and their associated Equivalent Series Resistance (ESR) loss [4].

2.3 **Multiphase Voltage Regulator Module**

The power management related issues become much more critical for future microprocessors and much more difficult to handle. To meet future microprocessor’s specifications, high efficiency, high power density, fast transient VRMs are required. To achieve these targets, the following technological challenges will have to be addressed:

1. Innovative integrated magnetics for low core losses, low winding losses and easy manufacturability for high efficiency and high power density [4]

2. Advanced VRM topologies to accommodate for high efficiency, high power density and fast transient response for low voltage, high current applications.

3. Optimization of multiphase VRM that provides a methodology for determining the appropriate number of channels and value of output inductance for the optimal operation of VRMs [6].

4. Advanced packaging technology to minimize parasitic which affects noise for high frequency operation [6].

5. Efficient synchronous rectification that incorporates new driving means or topologies to eliminate the body diode loss for high frequency operation [7].

In addition to above approaches, the performance of VRM may also be improved by increasing switching frequency. This is due to the fact that output ripple and dynamic response improve with increased switching frequency. The physical size and value of the filter inductor and capacitors
become smaller at higher switching frequencies. However, the switching losses increase with frequency, and the resulting efficiency may potentially be lower. The multiphase buck topology offers a solution to this problem. The fundamental operating switching frequency is effectively multiplied by the number of phases used, hence producing higher frequency effect at both input and output, and improving transient response.

2.4 Multiphase Buck Converter

![Figure 2-2 Multiphase Buck Converter](image)

Multiphase Buck topology uses the synchronous Buck topology as a building block. When two or more synchronous buck converters are put in parallel, they may form a multiphase converter called multiphase buck converter. In general, the multiphase buck topology puts $N$ number of buck converters in parallel. Each buck converter has a switching control signal with phase difference of $\frac{360}{N}$ degrees where $N$ is the phase number. So in case of the two phases, each phase control signal is shifted from each other by 180°. In the multiphase buck converter, duty cycle $D$ is the ratio of the output voltage $V_o$ and input voltage $V_{in}$ just like that in a regular buck converter. However, the main benefit of multiphase is the
current ripple cancellation effect which enables the use of the small inductance to allow faster transient response and smaller the output capacitance as explained later.

There are many advantages to using a multiphase buck over the synchronous buck. First, by increasing the number of phases, the effective frequency of input and output current increase. This allows for a faster transient response, and less filtering capacitors at both the input and the output. The output current frequency is the multiple of the number of phases times the switching frequency of each buck converter, i.e. \( f_{\text{Total}} = f \times N \). Secondly, each channel will carry less current due to multiple paths from input to output. This gives a major benefit especially in high current applications since conduction loss is proportional to current squared. This further means MOSFETs and inductors in the converter can be small, and need not to be too large. Furthermore, the temperature of the components will not be too high, improving efficiency which reduces heat sinking requirements. This in turn allows for greater power density of the converter. However, increasing the number of phase would increase complexity of the converter and component count which will raise the cost. To achieve a good compromise among efficiency, power density, and better dynamics, study suggests that a four phase multiphase buck topology gives the best case [8]. Therefore, the proposed VRM topology described in this thesis also focuses on a four phase configuration. The following sections discuss several VRM topologies aimed to improve the performance from the traditional VRM Buck topology.
2.5 Multiphase Phase-Shift Buck Converter (VRM)

![Figure 2-3 Multiphase Phase Shift Buck [9]](image)

The fundamental approach of the current VRM solution is by extending the duty cycle which may be done by the transformer. A transformer introduces the turns ratio \( n \), hence introducing an additional design variable allowing more desirable duty cycle. Among converters using the transformer concept, the Phase-Shift Full Bridge converter can extend the duty cycle as well as achieve soft switching which helps further in the reduction of the switching loss. The Phase Shift Buck (PSB) VRM converter uses an autotransformer and is shown in Figure 2-3 [9].

With phase-shifted control of the primary switches, zero voltage-switching turn-off of Q1-Q4 can be achieved. In the power transfer mode of the phase-shift buck converter, Q4 and Q3 are both on. In this mode Q6 is off and Qs is on for freewheeling. The one turn winding also serves as part of the current doubler. The autotransformer directly transfers some energy in addition to pure transformer coupling which is a more efficient way. By choosing the turns ratio, the duty cycle can be modified to achieve the higher efficiency. For example, with 12 V input, 1 V output, and \( n=2 \), the duty cycle will be 0.25. Again, the duty cycle is much higher compared to regular buck converter. While the multiphase phase-shift buck provides higher efficiency, it requires more devices in terms of switches and autotransformer, this will cost more. In addition, the use of transformer not only means increased loss,
but also increased volume and weight of the converter.

### 2.6 Digital Multiphase for CPU Power

![Digital Control on Multiphase Buck](image)

Figure 2-4: Digital Control on Multiphase Buck

A new method has been developed in order to meet the transient performance of Intel’s VRM 11.0 standard high slew rate requirements on future microprocessor power requires a minimization of parasitic line inductance that could affect voltage transient of sub 1 V logic gates [10].

The new method, as shown in Figure 2-4 uses Digital Multiphase Power (DMP) from Primarion/Intersil which changes controller architecture from an analog to a digital signal. This in turn offers flexibility, multi tasking, and noise immunity. The digital signal further allows the user’s access to a programmable control loop characteristics.

With the new method, each phase is time aligned resulting in a current ramp that is sum of all phase ramps. The architecture developed by Primarion/Intersil allows an operation up to 8 phases with 1 MHz switching frequency for each phase with a di/dt rates of 800 A/us on inductor and 1500 A/us on output capacitor [10].
2.7 Two Stage Approach VRM

![Diagram](image)

**Figure 2-5 Two Stage Multiphase Buck Diagram**

One approach to solve the duty cycle problem would be a two-stage multiphase buck converter as shown in Figure 2-5. A prototype for this type of circuit has been reported in [11]. A conversion from 12 V to 5 V is made on the first stage of the converter. A value of 5 V is selected as an intermediate bus voltage based on an optimization curve between bus voltages and switching frequency [11]. Another reason for the selection of this voltage is because 5V input has been an industry standard for many devices.

This type of design could be attractive since each stage may have high efficiency resulting in an improved overall efficiency of the converter. The duty cycle for the first stage and second stage would be equal to 41.67% and 20% respectively. An increase in duty cycle would reduce the peak current on the top MOSFET, thus increasing the overall converter's efficiency by lowering the switching losses on top MOSFET.
Another benefit of using this topology would be its ability to increase switching frequency on the second stage. Since the output voltage on first stage is 5 V, therefore switching loss would be reduce on the second stage compared to a direct conversion from 12 V input into 1 V output. It is proven in [11] that an increase in frequency corresponds to a reduced number of output capacitor required at the output of the converter. Unfortunately this type of topology only solves part of the problems that VRM designers are facing right now. Despite the obtained benefits, the topology suffers from slow transient response especially when switching at high load. Therefore, improvements should be explored with regard to the slow transient response.
Chapter 3. Proposed Multiphased Buck Converter

The proposed circuit for this thesis is shown in Figure 3.1. The topology utilizes interleaved switching for improved equal current sharing and better heat distribution. The circuit has 4 phases in a unique configuration. Every two buck converters are grouped together into one module whose output is connected to a Schottky diode $D_1$ to provide a shorter freewheeling path for inductor $L_5$ for the top module, and Schottky diode $D_2$ for inductor $L_6$ for the bottom module. Within each module, there are two individual synchronous buck converters connected in parallel. Each module is then connected to
other modules in parallel as well to allow the interleaving operation. Here MOSFETs Q1, Q3, Q5, and Q7 are being used as the top switches, which have the conduction time of DT, the product of Duty Cycle D and switching period T. Whereas MOSFETs Q2, Q4, Q6, and Q8 are being used as the lower switches with conduction time of (1-D)T. Both inductor-capacitor pairs of C1, C2, and L5 are the bypass components placed between input and output to increase the energy storage. Capacitor C2 is placed between the ground and the junction of individual output inductors L1 and L5. Similarly, capacitor C4 is placed between ground and the junction of individual output inductors L3 of the second module and the bypass inductor L6. This filter is used to provide a zero-ripple output current which in turn reduces the output capacitor rms current. This in turn reduces capacitor loss and lower rms rating of the capacitor.

![Figure 3-2 Timing Diagram for Top Mosfet](image-url)
Figure 3-2 shows the gate drive signals for each appropriate MOSFET. In multiphase multi-interleaving the sequence of turning on of switches is slightly different than that of a simple multiphase buck. To illustrate this, refer to Figure 3.1, where there are two modules, each consisting of two phases. MOSFET Q1 of module 1 which is assumed to be "phase 1" starts the timing signal. This switch is the first one to get turned on. After a delay of 90°, Q5 which is the top switch of "phase 2" in module 2, is next turned on. Then Q3 in "phase 3" of module 1 would turn on after a delay of 180° with reference to Q1. Lastly Q4 in module 2 and "phase 4" turns on after 270° delay from Q1.

![Figure 3-3 Equivalent Circuit in T₀ – T₁](image)

In steady state operation, when Q1, is turned on from T₀-T₁, the current flows from the voltage
source Vin to the load R through Q1, L1, and L5. The voltage across L1 is

\[ V_{L_{\text{sw, on}}} = L \frac{di_L}{dt} \]

consequently, the slope of its current is

\[ \frac{di_L}{dt} = \frac{V}{L_1} = \frac{Vin}{L_1} = \text{Constant.} \]

This means, the current through Q1 increases linearly since it equals the inductor L1 current, and also since input and output voltage are both fixed at 12 V and 1 V respectively. During this time, the energy stored previously in C1 is being discharged through Q1 and L1. While the energy stored previously in C2 is also being discharged through L5.

Figure 3-4 Equivalent Circuit in T₁ – T₂
Figure 3.4 corresponds to $T_1 - T_2$ when Q1 turns off and Q2 turns on. L1 was charged up when Q1 was on, and now it will be discharged through Q2, L5 to the load. Moreover, diode D1 conducts during this time period and energy stored in L5 flows to output. In the mean time current will also flow from C1 to the ground and result in charging it up. The energy in C1 would be charged by the input source during this time.

![Figure 3-5 Equivalent Circuit in $T_2 - T_3$](image)

Switch Q3 will be the next one to conduct in regular Multiphase interleaving technique. However in this proposed topology, switch Q5 conducts instead. One reason to do this is such that the heat sources from each MOSFET will be distributed more evenly compared with turning on Q3 first.
During this period $T_2$ to $T_3$, shown in Figure 3-5, the same sequence of energy flow occurs as the one described in the first phase (from $t_0$ to $t_1$). C3 replaces C1, C4 replaces C2, L3 replaces L1, L6 replaces L5, and D2 replaces D1. The same cycle will also repeat for sequence 3 (Q3 and Q4) and sequence 4 (Q7 and Q8).

3.2 Design Equation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>12 V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1 V</td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td>&lt; 15 mVP-p</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>40 A</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>&lt; 5%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>&lt; 2 %</td>
</tr>
<tr>
<td>Efficiency at Full Load</td>
<td>&gt; 80 %</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>500 kHz/phase</td>
</tr>
</tbody>
</table>

The important factors when choosing components were size, cost, and overall efficiency of the circuit. All components were chosen to be surface mount to reduce converter’s size and hence improving power density of the VRM. More importantly, the components have to be selected such that the proposed circuit meets the specifications listed in Table 3-1.
3.2.1 Inductor Selection

The most important values in order to determine the stability of the converter are inductance and capacitance values. In order to find the value of the output inductor in each phase, L1, L2, L3, L4, we will use: \( V_L = L \frac{di_L}{dt} \). Solving for \( L \), the equation becomes \( L = V_L \frac{dt}{di_L} \) where \( di = \Delta I_{LCH} \) is the ripple current through the output inductor of each channel.

Using \( dt = (1-D)T_s \) where \( T_s \) is the switching period, and \( D \) is the duty cycle, the inductor equation becomes \( L_{CH} \Delta I = V_{o}(1-D)T_s \).

The inductor current for each phase would be 10 A based on the requirements of 40 A full load and 4 phase buck converter. A 40 A full load was selected only as an example to test the functionality of the proposed multiphase buck topology. The actual multiphase buck that is used for VRM should run at least 100 A. For each phase, the minimum value for the inductance to maintain Continuous Conduction Mode for an average inductor current of 10 A is

\[
L_{MIN} = \frac{V_{OUT}(1-D)}{2f_{SW}I_{OUT}}
\]

\[
L_{MIN} = \frac{1*(1-\frac{12}{1})}{2*500*10^3*10} = 91.66 \text{ nH}
\]

According to Table 3-1, the minimum average load current required while the converter maintains CCM is 10 % of maximum phase current. This yields the inductor ripple current requirement of 10% * 10 A = 1 A. Hence:

\[
\Delta I_L = \frac{(V_BN - V_{OUT})}{L} * DT_s
\]
Solving for L yields:

\[ L = \frac{(12 - 1) \times \left(\frac{1}{12}\right) \times 2 \times 10^{-6}}{1} = 1.83 \text{ uH} \]

The maximum inductor current would be 10 A plus 0.5 A ripple based on our design choice. Therefore, the inductor should be able to withstand a total current of 10.5 A current without saturation and a low Direct Current Resistance (DCR) value in order to increase efficiency. Coilcraft inductor # MLC1260-172ML whose value is 1.75 uH was chosen in order to satisfy above conditions. This inductor has a peak current rating capability of 13.6 Ampere and a DC resistance value of 2.84 mΩ

### 3.2.2 Capacitor Selection

The input ripple current can be calculated by using Figure 3-6 [12].

![Figure 3-6 Input Ripple Factor](image)

The input rms current for capacitor can be found using this formula [12]:
\[ I_{\text{IN-RMS}} = \sqrt{A + B * [C + D]} \]

Where

\[ A = \left( D - \frac{k}{m} \right) \left( \frac{k + 1}{m} - D \right) I_o^2 \]

\[ B = \frac{m c^2}{12 m D^2} \left( \frac{V_o (1 - D) T}{L_f} \right)^2 \]

\[ C = (k + 1)^2 \left( D - \frac{k}{m} \right)^3 \]

\[ D = k^2 \left( \frac{k + 1}{m} - D \right)^3 \]

\[ T = \text{Period of each phase} \]

\[ m_c = \text{Number of channel} \]

\[ D = \text{Duty Cycle} \]

\[ m = \text{Number of phases} \]

\[ k = \text{Floor (m*D), m= 1,2,3,4,...} \]

The FLOOR function returns an integer value less than or equal to the expression inside the brackets. We can then calculate the worst case condition for capacitor input rms current at \( I_o \) equal to 40 A.

\[ A = \left( D - \frac{k}{m} \right) \left( \frac{k + 1}{m} - D \right) I_o^2 \]

\[ = \left( \frac{1}{12} - 0 \right) \left( \frac{0 + 1}{4} - \frac{1}{12} \right) 40^2 \]

\[ = 22.22 \]

\[ B = \frac{m c^2}{12 m D^2} \left( \frac{V_o (1 - D) T}{L_f} \right)^2 \]

\[ = \frac{4^2}{12 \times 4 \times \left( \frac{1}{12} \right)^2} \left( \frac{1 \times (1 - \frac{1}{12}) \times 2 \times 10^{-6}}{1.75 \times 10^{-6}} \right)^2 \]

\[ = 52.680 \]
\[
C = (k + 1)^2 \left( D - \frac{k}{m} \right)^3 \\
= (0 + 1)^2 \left( \frac{1}{12} - 0 \right)^3 \\
= 5.787 \times 10^{-4} \\
D = k^2 \left( \frac{k + 1}{m} - D \right)^3 \\
= 0^2 \left( \frac{0 + 1}{4} - \frac{1}{12} \right)^3 = 0
\]

Therefore: 
\[
I_{in\_rms} = \sqrt{A + B \cdot C + D} \\
= \sqrt{22.22} \\
= 4.71 \text{ A}
\]

Next we will be calculating the rms input current for a regular buck converter, then we can compare these two values of rms input current.

\[
A = \left( D - \frac{k}{m} \right) \left( \frac{k + 1}{m} - D \right) I_o^2 \\
= \left( \frac{1}{12} - 0 \right) \left( \frac{0 + 1}{1} - \frac{1}{12} \right) 40^2 \\
= 122.22
\]

\[
B = \frac{mc^2}{12mD^2} \left( \frac{V_s(1-D)T}{L_f} \right)^2 \\
= \frac{4^2}{12 \times 1^2 \left( \frac{1}{12} \right)^2} \left( \frac{1(1-\frac{1}{12}) \times 2 \times 10^{-6}}{1.75 \times 10^{-6}} \right)^2
\]
\[
210.72
\]
\[
C = (k + 1)^2 \left( D - \frac{k}{m} \right)^3
\]
\[
= (0 + 1)^2 \left( \frac{1}{12} - 0 \right)^3
\]
\[
= 5.787 \times 10^{-4}
\]
\[
D = k^2 \left( \frac{k + 1}{m} - D \right)^3
\]
\[
= 0^2 \left( \frac{0 + 1}{1} - \frac{1}{12} \right)^3 = 0
\]

Therefore:

\[
I_{IN\_RMS} = \sqrt{A + B \cdot [C + D]}
\]
\[
= \sqrt{122.22}
\]
\[
= 11.05\ A
\]

\[
I_{IN\_RMS} = \sqrt{\left( \frac{1}{12} - 0 \right) \left( \frac{0 + 1}{1} - \frac{1}{12} \right)^2 + \frac{4^2}{12 \times 1 \times \frac{1}{12}} \left( \frac{1(1 - \frac{1}{12}) \times 2 \times 10^{-6}}{1.75 \times 10^{-6}} \right)^2}
\]

\[
I_{IN\_RMS} = 11.05\ A
\]

Nichion Capacitor (PCF1D680MCL1GS 68uF/20V) was selected because by comparing these two rms input current, the multiphase buck converter reduces its current by 57%. The capacitor has an ESR value of 40mΩ and an rms ripple current rating of 2.6 A.
**Output Capacitor:**

The next component to design is the main output capacitor. The function of the capacitor is to hold the output voltage constant. In a real model of a capacitor, along with capacitance C there are two other associated quantities, namely the equivalent series resistance (ESR) and inductance (ESL). But at high frequency, ESR is more dominant than ESL and so ESL can be neglected. Based on our design Table 3-1, assuming an ideal capacitor is being used in the circuit, the minimum capacitance $C_{out}$ can be calculated for multiphase converter by:

$$C_{OUT} = \frac{(1-D)}{8Lf^2} \left( \frac{V_{OUT}}{\Delta V_{OUT}} \right)$$

$$C_{OUT} = \frac{\left( \frac{11}{12} \right)}{8(0.4375 \times 10^{-3})(2000 \times 10^{-3})^2 \left( \frac{1}{15 \times 10^{-3}} \right)}$$

$$C_{OUT} = 4.365 \text{ uF}$$

The value above is calculated assuming an ideal capacitor is being used in the circuit. An actual capacitor value should be higher considering capacitor’s ESR. An estimated value of output ripple voltage is then given by the following expression [12].

$$\Delta V_{O_{peak-peak}} < \frac{\Delta I_o T}{8(N)C_{OUT}} + \Delta I_o \times ESR$$

The first term on the equation with $\Delta I_o = \text{peak to peak output current ripple}$ calculates the output voltage ripple contribution from a pure capacitive component of the output capacitor ($C_{OUT}$). It can be seen also from equation above that a higher number of phases ($N$) will reduce this contribution value. On the other hand, the second part of the equation calculates the ESR contribution to the output voltage ripple. Assuming that we are using $C_{OUT}$ value of 4.365 uF and an output ripple current of 0.761 A calculated from previous equations, then the ESR value for output capacitor can be calculated:
\[
\frac{\Delta I_o T}{8(N)C_{\text{OUT}}} + \Delta I_o * \text{ESR} = 15 \text{ mV}
\]
\[
\frac{(0.761)(2 \times 10^{-6})}{8(4)(4.365 \times 10^{-5})} + 0.761 \times \text{ESR} = 15 \text{ mV}
\]
\[
10.89 \text{ mV} + 0.761 \times \text{ESR} = 15 \text{ mV}
\]

ESR = 5.4 m\Omega

The selection of output capacitor would be transient voltage overshoot during a step load change from full load to no load. The capacitance value can be calculated by equating inductive and capacitive energy [13].

\[
C_{\text{OUT}} = \frac{L * I^2}{V^2} = \frac{L_{\text{EQ}} * \left((I_{\text{FL}})^2 - (I_{\text{NL}})^2\right)}{(V_{\text{OUT2}})^2 - (V_{\text{OUT1}})^2}
\]

where

- \(L\) = effective inductance
- \(I_{\text{FL}}\) = Full Load Current
- \(I_{\text{NL}}\) = No Load Current
- \(V_{\text{OUT2}}\) = Maximum output voltage with overshoot
- \(V_{\text{OUT1}}\) = Nominal value for output voltage

Using 0.4365 \(\mu\)F as an effective inductance (\(L_{\text{eff}}\)), transient load current from 40 to 0 A and maximum output voltage with overshoot of 1.1 V then the required bulk capacitance needed can be calculated as follows:

\[
C_{\text{OUT}} = \frac{(0.4365 \times 10^{-6}) \times \left((40)^2 - (0)^2\right)}{(1.1)^2 - (0)^2} = 3333 \mu\text{F}
\]

The capacitance calculated above will limit an overshoot voltage of 100 mV when a load transition from 40 A to 0 A occurs. In order to meet this requirement, a number of capacitors with smaller values can be placed in parallel at the output of the converter. This method would also increase
converter’s efficiency because each capacitor handles a smaller value of output rms current while effectively reducing the overall ESR of output capacitance.

### 3.2.3 Output Current Ripple Cancellation

![Figure 3-7 Output Current Ripple](image)

Figure 3-7 shows the output current ripple normalized with inductor current ripple at varying duty cycle. We can calculate the exact value of output current ripple by:

\[
\Delta I_o = \frac{V_o(1-D)T}{L} \times \frac{N \left( D - \frac{m}{n} \left( m + 1 \right) \frac{1 - D}{n} \right)}{D(1-D)}
\]

where \( L \) is the inductance per phase of 1.75uH. \( T \) is period per phase of 2us. Plugging the design values for the proposed converter yields:

\[
\Delta I_o = \frac{1 \left( 1 - \frac{1}{12} \right) \left( 2 \times 10^{-6} \right)}{\left( 1.75 \times 10^{-6} \right)} \times 4 \left( \frac{1}{12} \right) \left( -0 \right) \left( \frac{0+1}{4} - \frac{1}{12} \right)
\]
\[ \Delta I_o = 0.761 \text{ A} \]

While regular buck converter, the peak to peak output current can be found by:

\[ \Delta I_o = \frac{V_o (1 - D) T}{L} \]

\[ \Delta I_o = 1.04 \text{ A} \]

The multiphase buck converter reduces the peak to peak current ripple by factor or 0.73. The rms output current ripple for output capacitor requirement can be calculated by

\[ I_{OUT, RMS} = \frac{I_{RIPPLE}}{\sqrt{12}} \]

\[ I_{OUT, RMS} = \frac{0.761}{\sqrt{12}} = 0.2196 \text{ A} \]

### 3.3 Duty Cycle

Duty cycle for the overall converter can be approximately calculated as:

\[ D = \frac{V_o}{V_{in}} = \frac{1}{12} = 0.0833 \]

Note that the calculated duty cycle is valid under steady state and continuous conduction mode condition.

### 3.4 MOSFET Selection

For the upper MOSFET, the dynamic or switching losses are the predominant factors, and conduction losses play secondary role because the duty cycle is very small and less than 10%. The conduction time is very small as compared to the number of switching from one state to another in one second. The MOSFET should meet the voltage and current specifications with as low a gate charge as possible to keep the dynamic losses small. Consequently, a MOSFET with a moderate \( R_{DS,ON} \) will be
desirable. For our MOSFET selection, a low $R_{\text{DS}-\text{ON}}$ MOSFET should be used for the synchronous or bottom or freewheeling MOSFET since this particular MOSFET conducts $11/12 = 91.67\%$ times out of the whole switching period. In order to increase converter’s efficiency, a proper value for gate to source voltage of the MOSFETs should be applied. A higher $V_{\text{GS}}$ would reduce $R_{\text{DS}-\text{ON}}$ for the MOSFET but it increases the total gate charged on each MOSFET. As mentioned above, a higher gate charge translates into a higher switching loss. Therefore a careful selection of gate to source voltage should be made in order to minimize MOSFET’s $R_{\text{DS}-\text{ON}}$ and the total MOSFET’s gate charge at the same time.

MOSFET FDS8690 for top MOSFET was chosen because of its low gate charge value of $10 – 14 \text{ nC}$ while MOSFET FDS6299S was chosen for the synchronous MOSFET because of its low $R_{\text{DS}-\text{ON}}$ of $3.9 \text{ m}\Omega$ and $Q_{\text{GD}}/Q_{\text{GS}}$ ratio of 0.727. These MOSFETs are from Fairchild Semiconductor.

### 3.5 Efficiency

![Efficiency vs Load](image)

**Figure 3-8 Efficiency vs Load Current**

Figure 3-8 depicts the calculated efficiency plot based on the design values and chosen parameter and component values calculated at varying load from 5A to 40A. As we can see from figure 3-8 that the expected maximum efficiency is approximately 84%. The same procedure was repeated.
over the full range of loads as graphed in Figure 3-8. Compared against the efficiency requirement listed in Table 3-1, the 84% efficiency at full load exceeds the requirement of higher than 80%. We can also observe from Figure 3-8 that the efficiency peaks up at mid range load followed by gradually decreasing efficiency due to I²R loss dominating the total loss.

Now that all the components have been selected and the efficiency has been calculated, we can proceed with simulation to test the proposed topology before a hardware prototype is built.
Chapter 4 SIMULATION

The proposed multiphase multi-interleave buck converter is simulated in Cadence Capture CIS. Figure 4.1 represents the open loop schematic of the multiphase multi-interleave buck converter. The input power supply is modeled by a constant voltage source $V_{in}$. The gate signals to the MOSFETs are generated by using $V_{pulse}$. The schematic is simulated for the runtime of at least 2ms to ensure the simulation reaches steady state. Each input and output capacitor’s ESR (Equivalent Series Resistance) along with inductor’s DCR (Direct Current Resistance) are also modeled in this simulation in order to get a good representation of the actual hardware circuit performance. Once the circuit schematic is completed, a transient analysis in OrCAD is run for at least 1 millisecond long to ensure steady state operation of the circuit has been reached. Circuit’s performance can then be studied by obtaining plots of critical parameters such as output voltage, inductor currents, output voltage ripple, etc.

It is important to note that components used in the schematic were modeled to be similar to the components purchased for the hardware prototype. The FDS8690 and FDS6299S MOSFET models were downloaded from Fairchild’s website, and so were the model for diodes MBR30455T. Another important note is that the duty cycle was adjusted manually to obtain an output voltage close to the value of 1 volt. This must be done due to the voltage drops in the circuit. If this was a closed loop system, then the duty cycle would be adjusted automatically by the controller. Finally, the load is modeled as a constant current source to mimic a constant current drawing of a load. Variation of the load is simply done by changing the value of the load current.
Figure 4-1 Open Loop Schematic Proposed Topology

4.1 Inductor Current

Figure 4-2 depicts the inductor current waveforms for phase 1 and 2. The switching frequency for each phase can also be calculated and its value is equal to \( \frac{1}{(974.004 \text{us} - 972 \text{us})} = 500 \text{ kHz} \) as expected.

Each inductor current needs to be checked in order to fully implement the cancellation factor on each stage. Inductor current for each phase has an average value of \( 40 \text{ A} / 4 = 10 \text{ A} \) and a peak to peak ripple value of 0.991 A. Phase shifting between phase 1 and 2 is verified by subtracting the time.
difference between peak inductor current of phase 1 and 2. The result is divided by a period of 2us and then multiplied by 360 degrees. In this case, the phase shift would be $90^\circ$.

![Figure 4-2 Inductor Current phase 1 & 2](image)

Figure 4-2 shows that inductor currents are being shared equally between the four phases.

A current ripple cancellation effect can be seen by a reduced value of peak to peak current ripple at this particular stage. Peak to peak current ripple is now 0.929 A. The current from each stage combines together on the output stage at the node right before the 35 mH inductor. These two currents will further add together at the node right before the output LC Filter, and produce low peak to peak output current ripple because of cancellation factor at each stage as shown in Figure 4-4. By comparing Figures 4-3 and 4-4, we can see that the peak to peak inductor current is being reduced from 40.416 to 39.631A. The final peak to peak current ripple is equal to 0.785A by subtracting 40.416A – 39.631A. Therefore, the output current ripple is about 79.2% from its initial value of 0.991A. Comparing this final value with the value of 0.761, a small difference was observed. This discrepancy is mainly caused by an output voltage that is slightly less than 1 V on the simulation. With an input voltage of 12 V and an actual
output voltage of 0.961 yields a duty cycle of $0.961 / 12 = 0.080$ instead of 0.0833. In addition, the waveform in Figure 4-4 also has a period of $\frac{1}{4}$ of that in Figure 4-3. This effectively shows the frequency multiplication effect of the multiphase.

Figure 4-3 Inductor current sharing in 4 phases

Figure 4-4 Output Current Ripple
4.2 Output Voltage Ripple

In Figure 4-5, the average output voltage at full load is 0.876 V with a peak to peak output voltage ripple value of 7.2 mV. This is less than the value specified on our design parameters of 15 mV.

We can also calculate the output ripple frequency from Figure 4-5:

\[
\frac{1}{(981.85\mu s - 980.685\mu s)} = 2 \text{ MHz}
\]

This value is very close to the expected value of 4 phases * 500 KHz = 2 MHz. This also shows the frequency multiplication effect of the multiphase topology.

4.3 Efficiency

Figure 4-6 shows that the input and output powers of the proposed multiphase converter are 38.64 W and 32.08 W respectively at full load 40 A. This corresponds to the full load efficiency of 32.08 / 38.64 = 83.02%.
The efficiency measurement at full load is shown in Figure 4-7. The full load efficiency passes the required or specified full load efficiency of 80%. In real hardware measurement, the efficiency may potentially be lower due to other losses not considered in simulation such as core losses, copper loss from the wiring, among others.
4.4 Review of Specifications

Table 4-1 Summary of Simulation Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage at 40 A</td>
<td>1 V</td>
<td>0.876 V</td>
</tr>
<tr>
<td>Output Voltage Ripple at 40 A</td>
<td>&lt; 15 mV&lt;sub&gt;pk-pk&lt;/sub&gt;</td>
<td>7.2 mV&lt;sub&gt;pk-pk&lt;/sub&gt;</td>
</tr>
<tr>
<td>Inductor Ripple Current per phase</td>
<td>1 A</td>
<td>0.991 A</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>&lt; 5%</td>
<td>N/A</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>&lt; 2%</td>
<td>N/A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt; 80%</td>
<td>83%</td>
</tr>
</tbody>
</table>

Table 4-1 shows the summary of simulation results compared with the calculated values. Also, notice that line and load regulations were not included since the simulation was tested as an open loop system or without feedback controller. As summarized in Table 4-1, simulation shows that all of the design specifications are met.
Chapter 5  Hardware

Once simulations were completed, a hardware prototype of the proposed topology was designed and built. Using ExpressPCB's software, the schematics and board layout were created. After soldering the components, the proposed Multiphase Interleaved Buck topology was ready to be tested. The schematic and layout for the PWM controller, MOSFET driver, and power stage of multiphase buck converter are shown in Figure 5-1, 5-2, and 5-3 respectively.

Figure 5-1 Schematic for TPS40091 Controller
Figure 5-2 Schematic of ISL6614 Driver

Figure 5-3 Output Schematic
5.1 Layout Guidelines

A couple of guidelines were followed during layout implementation of the design into a PCB board. First, the loop consisting of input capacitor, high side MOSFET and low side MOSFET has to be made as small as possible in order to minimize di/dt noise from switching. Therefore, depending on the inductance value from PCB trace, an induced voltage from di/dt switching can be reduced. The path of current along all of the above components was suddenly stopped during switching, causing an inductor current stop instantaneously. Since inductor current cannot change instantaneously, therefore its voltage will go up when di/dt is high.

The gate signals from each driver to MOSFET are also very sensitive to noise pickup. To prevent the noise, these gate signal traces are kept as short as possible to maintain the integrity of the signal itself. One good method would be running the gate drive signal in parallel with the PGND signal. In this case, the noise will be cancelled between the two traces because PGND trace carries a return path for gate signal. However, we need to be cautious of inductances on the traces as this might delay the gate signal from reaching MOSFET gate pin.

Feedback resistors for setting the output voltage have to be placed as close as possible to the feedback pin of the controller to reduce noise pickup that might caused the feedback to sense the wrong voltage at this pin. In order to ensure a steady input voltage, all bypass capacitors for the IC have to be made as close as possible into the input pin.

5.2 Test Equipment

The following lists test equipment used during hardware verification of the proposed multiphase buck topology. Two banana input jacks were placed to connect the board with an input voltage source. Since the design targets an output power of 40 Watts, therefore with an input voltage of 12 V, the
expected input current would be less than 4 A. Therefore, a regular banana to banana cable is sufficient to handle this much of current flowing from power supply into the board.

Since the input for driver chip is the same as input for the controller, then the MOSFET gate to source drive voltage would be the same as input voltage. One benefit of a high gate to source voltage is a lower MOSFET on resistance, which in turn reduces MOSFET conduction loss. Unfortunately, a high gate to source drive voltage will increase total gate charge supplied to the MOSFET during switching which will increase switching loss.

In order to check the current balancing between each phase, four current loops were added into the board. These current loops serve as test points for current probe amplifier. Verification of gate drive signals can be done by directly probing a dedicated PWM output from the controller.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>Hewlett Packard</td>
<td>6574A</td>
<td>DC Power Supply</td>
</tr>
<tr>
<td>GWInstek</td>
<td>GDS-2204</td>
<td>Digital Oscilloscope</td>
</tr>
<tr>
<td>GWInstek</td>
<td>GDM-8245</td>
<td>Digital Multimeter</td>
</tr>
<tr>
<td>RSR</td>
<td>M9803R</td>
<td>True RMS Multimeter</td>
</tr>
<tr>
<td>Tektronix</td>
<td>A6302</td>
<td>Current Probe</td>
</tr>
<tr>
<td>Hewlett Packard</td>
<td>HP 6060B</td>
<td>DC Electronic Load</td>
</tr>
</tbody>
</table>

Figure 5.4 shows a picture of the lab set up used for testing. Testing was done entirely in the Power Electronics Lab Building 20 Engineering East, Room 104. An important note while taking data is that the input power supply did not give an accurate reading of input voltage, nor did the voltage display on the electronic load for the output voltage. Therefore, multimeters were utilized to measure the
correct input voltage and current and the correct output voltage. Also, for more accuracy, both input and output voltages were measured directly from their corresponding terminals on the board.

Figure 5-4 Testing Set up

5.3 Testing Results

5.3.1 PWM Gate Signals

Figure 5-5 shows the PWM signals which are at approximately 482 kHz and are interleaved as desired. Each phase in this proposed topology is shifted by 90 degrees. The duty cycle for the buck converter with input voltage 12 V and output voltage 1 V is 0.0833. This corresponds to a time difference between Phase 1 and Phase 2 of 520 ns which is equal approximately to 90 degrees based on 520 ns / 2us * 360 degrees.
Figure 5-5 PWM Gate Signal

Figure 5-6 the time difference between Phase 1 and Phase 3 is 1.040 us, which is equal approximately to 180 degrees based on 1040 ns / 2us * 360 degrees. Likewise, Figure 5-7 shows the time difference between Phase 1 and Phase 4 is 1.560us, which is equal approximately to 270 degrees based on 1.560 us / 2us * 360 degrees.
As shown in the previous figures, the PWM signals are at approximately 482 kHz and are interleaved as desired. The switching frequency is not exactly 500 kHz because the timing resistor used was not the exact value calculated to achieve 500 kHz. To achieve the exact value of 500 kHz, the resistor used would have to be a non-common resistor value of 53.76 KΩ. Therefore, the only common value closest to the exact resistor was used which is 53.6 KΩ. This resistor is connected between pin 16 and ground at TPS40091 PWM Controller.

### 5.3.2 Inductor Currents

Based on the calculation done in Chapter 3, the expected value for peak to peak inductor current for each phase is 1 A. Figure 5-8 shows Peak to Peak Inductor Current Ripple with a current probe amplifier set with a ratio of 10 mV equal to 0.5 A. Therefore a 20 mV peak to peak voltage ripple corresponds to a 1 A peak to peak current at each phase inductor current. The inductor currents of Figure 5-8 are shown at low load condition. Figure 5-5 also shows that the low side MOSFET is turned on...
during light load condition. Therefore, there would be some power loss during the turn on and off from this low side MOSFET.

![Figure 5-8 Peak to Peak Inductor Current](image)

**Figure 5-8 Peak to Peak Inductor Current**

Figure 5-9 indicates that the inductor currents are not equally shared between each phase. This unequal sharing may be explained by the fact that the current for each phase is sensed by the PWM controller using the DCR current sensing method. Therefore, a small noise on the sensing traces might have affected the controller current sharing capability. Thermal variations of inductor’s copper resistance also might affect the current balancing function of the PWM controller. Thermal variations of inductor’s copper resistance also might affect the current balancing function of the PWM controller. Another possibility of the current balancing error is that the controller needs a common node for sensing all 4 inductor currents. With the proposed multiphase topology, this common node is hard to find since inductor current for 2 phases is connected with an auxiliary inductor before going into the output.
5.3.3 Output Voltage Ripple

Figure 5-10 depicts the waveform of output voltage peak to peak ripple. It also shows the output voltage ripple with a load current of 3A after limiting the bandwidth of the scope to 20 MHz and a digital noise filter of 1.5 bits. The proposed multiphase topology should have a low peak to peak output voltage ripple. The waveform is not very clean due to noise on the output. One possible noise source would be the induced $dv/dt$ turn-on of the high side MOSFET. This can be shown by a rectangular pulse every 500 ns which equals to the delay between each phase. A layout improvement should be made to reduce the effect of this noise by either minimizing the loop between the input capacitor, high-side MOSFET, low-side MOSFET or by isolating this noise power ground from signal ground. The peak to peak output voltage ripple can be approximated around 8 mV if the switching noise were excluded from the picture. This value can be verified to be lower than the required value of 15mV from Table 3-1. The output ripple period can also be verified from Figure 5-10 above which is equal to 500 ns or a frequency...
of 2 MHz. The value is expected from a multiphase buck converter which has 4 phases with each phase running at a switching frequency of 500 kHz as expected.

![Figure 5-10 Output Voltage Ripple](image)

### 5.3.4 Transient Response

Another part of testing would be to monitor the output voltage during load transient. During step up load transient, the output voltage would momentarily droop when the output current is raised. The droop is caused by the inability of inductor to handle the entire inrush current. Therefore, output bulk capacitors were put in order to help supply charges to the output and maintain the output voltage at the same level. If there is not enough charge to supply the increased demand of current, then the output voltage will momentarily droop before the high gate turns on again to restore the output voltage.

The opposite effect occurs during step down load transient. The output voltage would momentarily go up due to sudden loss of load. In this case, the capacitor prevents the stored energy in inductor to discharge to the output.
In summary, the function of output bulk capacitor is mainly to maintain the output voltage to within regulation limits during load transient.

A load transient from 0 to 15 A was applied from the proposed multiphase buck output terminal as depicted in Figure 5-11. The slew rate for current step was 0.33 A/μs due to limitations of HP6060B Electronic Load. A higher value for current slew rate will increase the amount of overshoot and undershoot of output voltage during this transient response. As shown in Figure 5-11, the voltage overshoot and undershoot were 65.1 mV and -78.3 mV. The duration for these transients are approximately 160 μs for overshoot and 120 μs for undershoot before the output voltage reaches its steady state value. These overshoot and undershoot values can be reduced by increasing the control loop bandwidth of the converter.
5.3.5 Load Regulation

To test the load regulation, the minimum load was imposed at 0 A (or open), while full load was chosen to be at 40 A as specified by the design requirement. The nominal output voltage is 1 V. The load regulation, as commonly defined, equals to a change of output voltage with a load variation from no load to full load while input voltage is at nominal value (12 V in this case). For the proposed topology, the following was measured:

\[
\text{Load Regulation} = \frac{V_{\text{OUT(No Load)}} - V_{\text{OUT(Full Load)}}}{V_{\text{OUT(Full Load)}}} \times 100\%
\]

\[
= \frac{1.0089V - 0.9968V}{0.9968V} \times 100\%
\]

\[
= 1.2\%
\]

This means the load regulation of the proposed topology meets the specification for load regulation which was set to be less than 2%.

5.3.6 Line Regulation

Line regulation measures a change of output voltage compared to nominal output voltage at full load when the input voltage is varied from minimum to maximum value as defined by the requirements. In this project, the minimum input voltage is defined to be 10 V while the maximum is defined at 14 V.

\[
\text{Line Regulation} = \frac{V_{\text{OUT(High Input)}} - V_{\text{OUT(Low Input)}}}{V_{\text{OUT(Nominal)}}} \times 100\%
\]

\[
= \frac{0.9968V - 0.9967V}{1.008} \times 100\%
\]

\[
= 0.01\%
\]

This shows that the line regulation of the proposed topology meets the line regulation specification of less than 5%.
5.3.7 Efficiency

After testing the prototype through line and load regulations to ensure that no major problems were encountered, the efficiency of the hardware prototype was taken to compare against simulated and calculated values.

Figure 5-11 shows the measured overall efficiency for the proposed topology. The figure shows the overall efficiency of the circuit is plotted against the output current. The output current is varied from 0 A to 40 A. There is a maximum current limit that can be drawn by using an electronic load. This is based on the voltage at its terminals because the converter has to run with a low voltage of 1 V and high current of 40 A. Once the load terminal voltage drops into approximately 0.3 V, no more current can be drawn by the load. The load terminal drops because of the voltage drop across the wire that connects between the load and converter. Hence, a second electronic load was used in parallel with the first one to draw more current out of the converter. Once the first load has reached its maximum current, then the second load is set to start drawing current in order to achieve a maximum load of 40 A.

![Efficiency Curve](image)

Figure 5-12 Efficiency VS Load Current
Maximum efficiency from hardware measurement yielded a value of 77.97%. This is lower than both the calculated and simulated values. Moreover, the hardware efficiency does not meet the required efficiency of > 80%. This may be due to other losses that were not calculated or modeled in the simulation such as core loss and copper loss of the inductors as well as the gate drive losses.

Table 5-2 summarizes results of the proposed topology from simulation and hardware against the design specifications. As can be seen in Table 5-1, all specifications were met by the simulation and experimentation of the proposed topology except for efficiency. However, the efficiency was an improvement upon that of the previous Cal Poly topology which had an efficiency of 52.985% [8]. In this sense, the proposed topology has accomplished the goal of improving efficiency from the previous topology. However, the desired efficiency of 80% at full load was not met. Overall, the proposed topology is successful in meeting the expectations for use as a Voltage Regulator Module.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Simulation Result</th>
<th>Hardware Result</th>
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<tr>
<td>Input Voltage</td>
<td>12 V</td>
<td>12 V</td>
<td>12 V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1 V</td>
<td>0.876 V</td>
<td>0.9968 V</td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td>&lt; 15 mVpk-pk</td>
<td>7.2 mVpk-pk</td>
<td>8 mVpk-pk</td>
</tr>
<tr>
<td>Output Current</td>
<td>40 A</td>
<td>40.47 A</td>
<td>40 A</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>&lt; 5%</td>
<td>N/A</td>
<td>0.01%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>&lt; 2%</td>
<td>N/A</td>
<td>1.2%</td>
</tr>
<tr>
<td>Efficiency at full load</td>
<td>&gt; 80%</td>
<td>83%</td>
<td>77.97%</td>
</tr>
</tbody>
</table>
Chapter 6 Conclusion

6.1 Summary

According to Moore's Law, the number of transistors in a computer doubles every two years. The increase in the number of transistors means that more power will be consumed by the microprocessor. According to International Technology Roadmap for Semiconductors, the requirement for power is increasing by low per year since 2001 for high performance CPU To reduce the power losses the power supply voltage will be around 0.7 V and the current demand will be 170A in year 2010 [2]. In order to provide power at this level to future microprocessors, a dedicated power supply called Voltage Regulator Module (VRM) is needed.

With the current VRMs topology of synchronous buck, serious technical challenges contribute to decreased power density and increased cost. These technical challenges are: very small duty cycle, high switching frequencies, higher current demands, fast transient response. The proposed Multiphase Multi-Interleaved buck topology was designed in order to solve some of these technical challenges.

This thesis paper focused primarily on the efficiency improvement of the previous hardware prototype, reduction its board size to approximately 50% and to proper implementation of multiphase and interleaving control signals. By careful selection of MOSFET and a fast MOSFET driver, we can indeed improve the efficiency of the converter by approximately 25% at full load of 40 A. As presented in this report, the proposed topology met the design goals of an interleaved switching in addition to meeting the specifications that were laid out in Chapter 3. Overall, the proposed topology was successful.
6.2 Future Work

There are a few improvements to the proposed topology that could improve efficiency. First, we should find capacitors with even lower ESR. The ESR creates problems associated with power loss which degrades efficiency of the converter. Organic polymer capacitors provide high capacitance at low ESR; though, they are more costly than electrolytic capacitors. Another way to improve efficiency is to decrease the RMS input current. This translates to reduction of loss in major components such as the MOSFETs, inductors, and capacitors. Furthermore work can be done on improving the efficiency and load regulation by selecting more appropriate and less resistive components.

The board size may also be reduced by tightening the trace design and by eliminating the loops currently used for measuring inductor current. Finally, a finalized board should be designed to interface directly with microprocessors as done commercially so the performance of the proposed topology may be compared against those of the commercially available VRMs.
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APPENDIX

TOP LAYER
INNER GROUND LAYER
<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturers Name</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C2</td>
<td>Polymer Aluminum, 68uF, 20V, 40 mohm, 20%</td>
<td>Nichion</td>
<td>PCF1D680MCL1G5</td>
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<td>C3 - C6, C8, C18, C19, C26, C27, C30, C31</td>
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<td>Kemet</td>
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<tr>
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<td>MLC1260-172ML</td>
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<tr>
<td>L5-L8</td>
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</tr>
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<tr>
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<tr>
<td>U1</td>
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<td>TPS40091PWR</td>
</tr>
<tr>
<td>U2, U3</td>
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<td>Intersil</td>
<td>ISL6614</td>
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<tr>
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<tr>
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<td>RK73H2BTTD10R0F</td>
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<tr>
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<td>R10-R13</td>
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<tr>
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