

Effect of Gold Content on the Reliability of SnAgCu Solder Joints

Jianbiao Pan,

Julie Silk, Mike Powers, and Patrick Hyland

Abstract—Electroplated Ni/Au over Cu is a popular metalization for printed circuit board finish as well as for component leads, especially wire-bondable high-frequency packages, where the gold thickness requirement for wire bonding is high. The general understanding is that less than 3 wt% of Au is acceptable in SnPb solder joints. However, little is known about the effect of Au content on the reliability of SnAgCu solder joints. The purpose of this paper is to determine the acceptable level of Au in SAC305 solder joints. Three different package platforms with different Au thicknesses were assembled on boards with two different Au thicknesses using a standard surface mount assembly line in a realistic production environment. The assembled boards were divided into three groups: as-built, isothermally aged at 125 °C for 30 days, and isothermally aged at 125 °C for 56 days. All boards were then subjected to accelerated mechanical reliability tests including random vibration and drop testing. The results show that solder joints with over 10 wt% Au are unacceptable. If Cu is available to dissolve in the solder joint, then an Au content under 5 wt% will not significantly degrade the reliability of the solder joint. When Ni layers are present on both the board and the component sides of the interface, this limits the ability of Cu to dissolve into the solder joint, and hence an Au content under 3 wt% is acceptable. The failure mechanism for solder joints with high Au content is fractures through the AuSn₄ intermetallic compound. Additional findings confirmed that there is a danger of placing parts near high-stress areas and that a high level of voiding reduced reliability.

I. INTRODUCTION

ELECTROPLATED Ni/Au over Cu is a popular metalization for printed circuit board (PCB) surface finish as well as for component leads. The Ni layer functions as a diffusion barrier layer. The Au layer is used to: 1) protect the Ni layer from oxidation and corrosion; 2) enhance the soldering wettability; and 3) improve wire bondability in some applications.

During the soldering process, Au dissolves into the molten solder very quickly. It has been reported that molten Sn can erode a nominally 25- μ m-thick layer of Au in 10 s at 235 °C

[1] and the dissolution rate of Au in Sn40Pb (60 wt% Sn and 40 wt% Pb) solder is as high as 4.2 μ m/s at 252 °C [2], [3]. At such a rapid dissolution rate, all Au in a PCB and component lead, which has typically less than 0.8 μ m of Au, will be dissolved in a typical lead-free reflow profile where the time above liquidus is generally 30–90 s. When the solder joint solidifies, a brittle AuSn₄ or (Au, Ni)Sn₄ intermetallic compound (IMC) is formed in the solder joint. The presence of brittle AuSn₄ or (Au, Ni)Sn₄ IMC in the solder joint raises concerns about reliability.

The current understanding about the failure mechanism of “Au embrittlement” is as follows: when the solder joint solidifies during the soldering process, brittle AuSn₄ or (Au, Ni)Sn₄ IMC is formed in the bulk solder joint. After aging, the AuSn₄ migrates to the Ni interface and forms a continuous layer of (Au, Ni)Sn₄ IMC over the Ni₃Sn₄ IMC layer. The weak interface between (Au, Ni)Sn₄ and Ni₃Sn₄ results in brittle interfacial failure [4]. The driving force for the migration of AuSn₄ is a reduction of energy by mixing. Gold seeks Ni so that AuSn₄ becomes a Ni-saturated (Au, Ni)Sn₄ compound [4]. It has been reported that the thickness of the Ni layer has a significant effect in Au embrittlement as well. Alam *et al.* [5], [6] found that a thin layer of Ni facilitates the diffusion of Cu into the (Au, Ni)Sn₄-solder interface and changes the (Au, Ni)Sn₄ layer to a (Au, Cu, Ni)₆Sn₅ layer. They explained that the elimination of the brittle layer of (Au, Ni)Sn₄ IMC over the Ni₃Sn₄ layer prevents cracks from propagating along the interface between (Au, Ni)Sn₄ and Ni₃Sn₄. Though a thin Ni layer has this benefit, in practice, a thin Ni layer may limit the shelf life and solderability of PCB.

Less than 3 wt% of Au is considered to be acceptable in SnPb solder joints. A comprehensive study was conducted by Glazer *et al.* [7]. They investigated the effect of Au content on the long-term reliability in the defined service environment of SnPb solder joints between a plastic quad flat pack component and a PCB with Ni/Au finish and concluded that 3.0 wt% of Au is acceptable. However, little is known about the effect of Au content on the long-term reliability of SnAgCu solder joints. The objective of this paper is to fill this void.

There are two differences between a eutectic SnPb solder and a SnAgCu solder on the dissolution of Au and their effect on the reliability of solder joints. One is the high-Sn content effect. The Sn content in Sn3.0Ag0.5Cu solder is 96.5 wt% and that in eutectic SnPb solder is 63 wt%. Intuitively, a solder with higher Sn content should be able to take more Au to form AuSn₄ IMC. Chang *et al.* [8] also found that the migration kinetics of AuSn₄ to the solder-pad interface during thermal

aging in high-Sn solders was slower compared to that in eutectic PbSn. The other is the Cu effect in the SnAgCu solder. Shiau *et al.* [9] showed that 0.5 wt% of Cu can reduce the Ni consumption rate in solder joints with an Ni/Au surface finish.

In this paper, we report on a comprehensive study regarding the effect of Au content on the long-term reliability of SnAgCu solder joints in three different package platforms on PCBs with an Ni/Au surface finish. First, the Au content in the final solder joint is calculated based on the measured solder paste volume and the measured Au thickness in the PCB surface finish and/or the component surface finish. The assembled boards were divided into three groups: one without any thermal treatment, one isothermally aged at 125 °C for 30 days, and the third group aged at 125 °C for 56 days. All three groups were subjected to long-term mechanical reliability testing including random vibration and mechanical shock. The reliability test plan was based on Agilent’s typical industrial instrument operation environment. The reliability data are reported. Furthermore, the failure locations and mechanisms are presented.

II. METHODOLOGY

A. Component, Test Vehicle, and Assembly Process

The test vehicle is shown in Fig. 1. The PCB employed has six layers and is made of Nelco N4000-12. The board finish is electrolytic Au over Ni. There are two different Au thicknesses: a flash Au finish with 0.08–0.38- μm Au over 5- μm Ni, and a thick Au finish with 2–2.54- μm Au over 5- μm Ni. Five types of components were assembled on the test vehicle. All components were daisy-chained. The package information is summarized in Table I. There are nine quad flat no-lead 5 (QFN5) packages, nine QFN6 packages, nine TOPS packages, six FP I packages, and six FP II packages per board. All components have underbelly pads.

The assembly process was done using a standard surface mount assembly line in a realistic production environment. The solder paste used is Sn3.0Ag0.5Cu (SAC305) Type 3 with no-clean flux and a metal content of 88% by weight. The stencil used is electroformed Nickel, laser cut with a foil thickness of 0.1 mm (4 mils) and 1:1 aperture to pad ratio. The volume, area, and height of solder paste on each pad of each board were measured by a solder paste inspection system. The reflow process was done in nitrogen and the reflow profile is shown in Fig. 2. After assembly, the resistance of every daisy chain was measured and documented. All solder joints were inspected using 2-D X-ray. Any defects related to the assembly such as missing wire bonds in the component, insufficient solder, or bent leads were documented.

B. Reliability Testing

The assembled PCBs were randomly divided into three groups as shown in Table II. The boards in Group 1 were not subjected to thermal aging. The boards in Group 2 were subjected to isothermal aging at 125 °C for 30 days. The boards in Group 3 were subjected to isothermal aging at 125 °C for 56 days. The isothermal aging at 125 °C for 0 h,

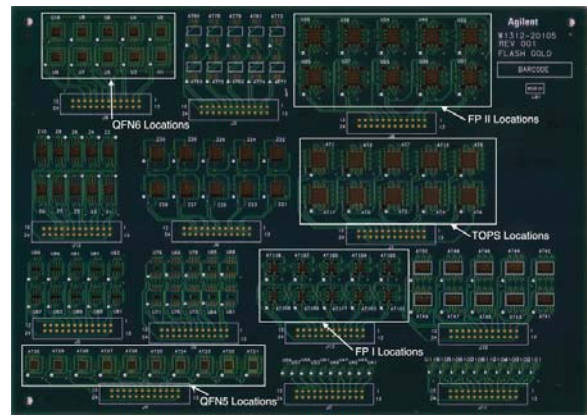


Fig. 1. Test vehicle.

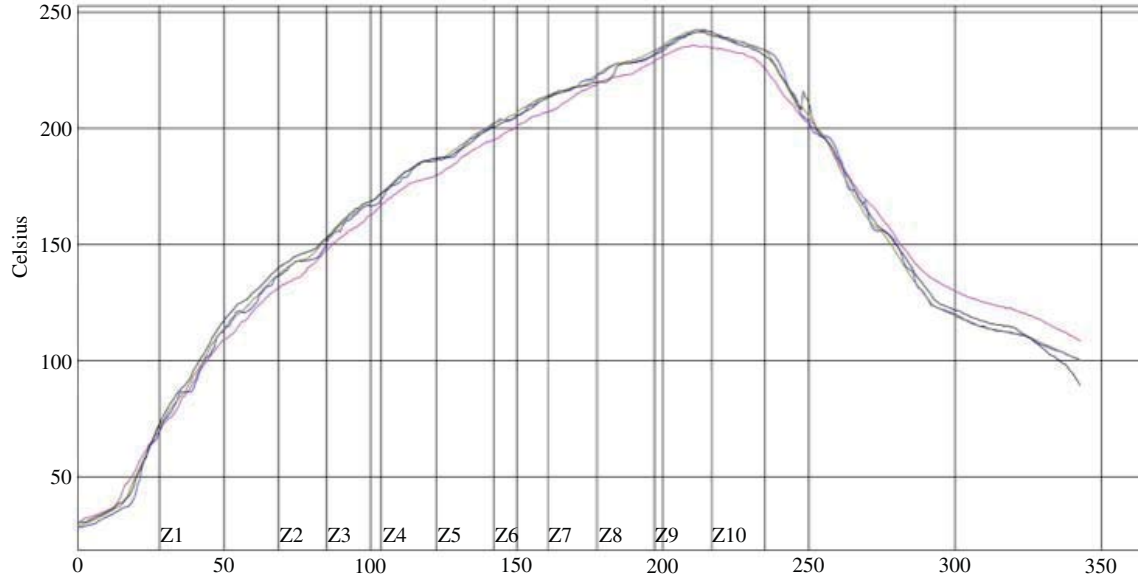
TABLE I
SUMMARY OF PACKAGES

Package Type	Number of Packages per Board	Package Size and Type	Lead Material	Lead Finish
QFN5	9	5 mm × 5 mm Quad flat no lead	Cu	Matte Sn
QFN6	9	6 mm × 6 mm Quad flat no lead	Cu	Matte Sn
TOPS	9	10 mm × 10 mm RF laminate, open cavity, no lead	Cu	0.28–0.46- μm Au over 3.8–8.5- μm Ni
FP I	6	6.4 mm × 6.4 mm Ceramic, open cavity, flat leads	Kovar	1–2- μm Au over 1–5- μm Ni
FP II	6	10.2 mm × 9.7 mm Ceramic, open cavity, flat leads	Kovar	1–2- μm Au over 1–5- μm Ni

30 days, and 56 days was to simulate a reliability life of 0, 7, and 14 years when devices operate at 60 °C.

All boards were subjected to mechanical reliability testing. Each mechanical reliability test cycle includes: 1) random vibration at power spectral density (PSD) of 0.002868 g^2/Hz (0.275 m^2/s^3), 5–120 Hz for 50 minutes, and 2) mechanical shock at 250 G, 2.3-ms duration for 10 drops. Random vibration is chosen instead of sinusoidal vibration because it has been shown that random vibration more closely represents the true environment [10]. In the vibration testing, it is important to select two key parameters: frequency range and PSD level, because the reliability of solder joints on a board is mainly determined by these two parameters. It is advised that the test frequency range should include the natural frequency of the test board, because at this frequency, the board will experience the highest displacement, which generates highest stresses on solder joints. The natural frequency of the test vehicle was measured at 61 Hz. The acceleration level of this random test is 0.57 G root mean square (RMS), which is calculated by the square root of the area under the random vibration curve, or $\sqrt{0.002868 \text{ G}^2/\text{Hz} \times (120 - 5)\text{Hz}}$. The acceleration level of 0.57 Grms is around two times the typical vibration profile (in the range between 0.20 and 0.35 Grms) that products experience in transport as specified [11].

Setpoints (Celsius)										
Zone	1	2	3	4	5	6	7	8	9	10
Top	150.0	165.0	170.0	200.0	220.0	230.0	240.0	250.0	265.0	230.0
Bottom	150.0	165.0	170.0	200.0	220.0	230.0	240.0	250.0	265.0	230.0
Conveyor Speed (inch/min): 36.01										



PWI = 81%	Max Rising Slope		Max Falling Slope		Soak Time 150–217°C		Reflow Time/217°C		Peak Temp	
U22 PIN10	2.00	25%	-1.77	49%	87.09	81%	65.71	12%	236.12	-54%
AT1 PIN23	2.51	57%	-2.12	26%	84.63	64%	73.78	41%	242.62	18%
AT1 GND	2.33	45%	-2.19	20%	84.79	65%	75.15	46%	242.83	20%
U18 GND	2.47	54%	-2.42	5%	86.34	76%	74.67	44%	241.56	6%
Delta	0.51		0.65		2.46		9.44		6.71	

Fig. 2. Reflow profile used in this paper.

TABLE II
NUMBER OF BOARDS UNDER RELIABILITY TESTING

	Cross-sectioning & SEM/EDX		Mechanical Reliability	
	Flash Au	Thick Au	Flash Au	Thick Au
Group 1: no aging	1	1	6	6
Group 2: thermal aging for 30 days at 125 °C	1	1	5	6
Group 3: thermal aging for 56 days at 125 °C	1	1	5	6

Equation (1) is used to estimate the vibration fatigue life [10]

$$T_1 G_1^b = T_2 G_2^b \quad (1)$$

where T is life time, G is the acceleration in RMS, and b is the fatigue exponent. In this paper, we assume the fatigue exponent b is equal to 4 for leadless or flat lead parts at a printed circuit assembly level. Note that the vibration fatigue exponent for aluminum leads has been specified as 6.4 [10]. Military standard MIL-STD-810G specifies 7.5 and mentions

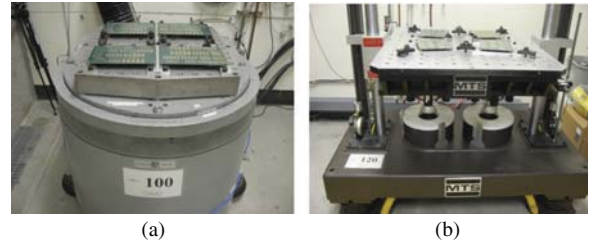


Fig. 3. Setup of the random vibration and the drop test. (a) Random vibration setup. (b) Drop test setup.

a range of 5–8 for fatigue exponent [12]. Thus, our estimation is more conservative. The vibration for 500 mins in this paper simulates the real vibration life of

$$T_1 = T_2 \left(\frac{G_2}{G_1} \right)^b = 500 \times 2^4 = 8000 \text{ minutes} = 133 \text{ hours.}$$

The setups for the random vibration and the drop tests are shown in Fig. 3. The board was placed in a horizontal orientation with components facing in a downward direction, which results in maximum board deflection. All boards were subjected to 10 cycles of random vibration, or 500 mins total, and 100 drops.

The resistance of each daisy chain was measured by an Agilent 34970A data logger with three 34901A 20-channel multiplexers and one 82357B USB/GPIB interface. Note that

Agilent data logger 34972A or 34980A can be used as well. The resistance measurement was done after each vibration test cycle (50 mins) or each drop-test cycle (10 drops).

C. Failure Criteria

Although solder joint reliability has been studied for over 30 years, the failure criteria are still not well defined and the relationship between the crack area of an interconnection and the change in resistance of the interconnection has not been established. Thus, different researchers use different failure criteria, for example, a resistance threshold of 450 Ω [13], an increase in resistance of 10 Ω or greater [14], a resistance change of 5 Ω [15], a resistance threshold of 100 Ω or 20% increase in resistance if initial resistance is over 85 Ω [16], and a resistance threshold of 1000 Ω [17]. In a sense, all of these criteria are subjective, because at this time no scientific research has been done on the interconnection failure criteria. Henshall *et al.* [18] compared three different electrical failure criteria, 20% resistance rise, 500 Ω , and hard open (infinite resistance), and concluded that the use of the IPC-9701A standard failure criterion of 20% resistance rise provides the most sensitive measure of failure among those studied.

In this paper, the failure criterion is defined as an increase in resistance of 2 Ω or more from initial resistance. Our principles for establishing this criterion are: 1) to detect solder joint failure as early as possible, and 2) no fault detection due to measurement error/variation. The initial daisy chain resistances in this paper are between 0.75 and 2.83 Ω . We did a gauge repeatability and reproducibility (GR&R) study on the data acquisition system (Agilent data logger 34970A) and concluded that the 3 sigma of the data acquisition system was $\pm 0.6 \Omega$. The failure analysis based on the cross-section and scanning electron microscope (SEM) analysis confirmed that a full crack in the solder joint had occurred if the change in resistance was 2 Ω . The details of this GR&R study and the relationship between the crack size and the change of resistance will be reported in a future paper.

III. RESULTS AND DISCUSSION

To compare the reliability of solder joints with different Au contents, it is important to calculate the Au content in the final solder joint. Since there is variation in Au thickness at different locations on a board, on different boards, and on different component leads, and since there is variation in solder paste volume of a package type on different pads and different boards, the mean and standard deviation of Au content were calculated. We also found that the SAC solder wetted the tops of gold-plated leads, increasing the gold that entered the solder joint. All Au on the wetting area of the PCB pad and the component was dissolved in the solder joint as verified by the SEM/energy dispersive X-ray (EDX) analysis. In this project, the calculation of the Au content is based on the measured solder paste volume and the measured Au thickness on the PCBs and on the components.

TABLE III
AU CONTENT IN WEIGHT PERCENTAGE IN SOLDER JOINTS

		QFN5	QFN6	TOPS	FPI	FPII
Flash Au board	Mean	0.5	0.5	2.5	15.0	11.8
	Standard deviation	0.15	0.15	0.3	2.5	2.2
Thick Au board	Mean	4.2	4.0	5.5	16.0	13.7
	Standard deviation	1.3	1.2	1.2	2.5	2.2

The volume of solder paste on every pad of every board was measured by a solder paste inspection system. The Au coating thickness on the component and on the board was measured by an X-ray fluorescent system on sample locations. The Au content in the solder joint is calculated according to (2), where:

Au weight in component = (area of component lead wetted by solder paste) \times (Au thickness on component lead) \times (density of Au);

Au weight in PCB = (area of pad) \times (Au thickness on PCB) \times (density of Au);

SnAgCu weight in paste = (measured solder paste volume) \times (metal content in volume) \times (density of SAC305).

For example, the FP I component lead is 0.254-mm (10-mil) wide and 0.152-mm (6-mil) thick, and the wetted length of the lead is 0.66 mm (26 mils). Thus, the area of component lead wetted by solder paste is 0.536 mm² (0.254 \times 0.66 \times 2 + 0.152 \times 0.66 \times 2). The mean and standard deviation of measured Au thickness on the component lead are 1.71 μm and 0.25 μm , respectively. Thus, the mean and standard deviation of Au volume on the component is 9.15 $\times 10^{-4}$ mm³ and 1.32 $\times 10^{-4}$ mm³, respectively. The pad size on PCB is 0.66 \times 0.41 mm. The mean and standard deviation of measured Au thickness on the PCB with flash Au are 0.098 μm and 0.029 μm , respectively. Thus, the mean and standard deviation of Au volume on the PCB are 2.65 $\times 10^{-5}$ mm³ and 7.80 $\times 10^{-6}$ mm³, respectively. The mean and standard deviation of measured solder paste volume of the FP I component on the flash Au board are 0.028 mm³ and 0.0028 mm³, respectively. Since the metal content is 50% in volume, the mean and standard deviation of SnAgCu volume of the FP I component on the flash Au board will be 0.014 mm³ and 0.0014 mm³, respectively. The density of Au is 19.32 g/cc and the density of SAC305 is 7.36 g/cc. Using the Monte Carlo simulation method, we get the Au content of FP I component on the board with flash Au with a mean of 14.9 wt% and a standard deviation of 2.6 wt%. The calculated mean and standard deviation of Au content data in weight percentage are summarized in Table III. It shows that there is a wide range of Au content between these five package types on two types of boards.

$$\text{wt\%Au} = \frac{\text{Au weight in component} + \text{Au weight in PCB}}{\text{SnAgCu weight in paste} + \text{Au weight in component} + \text{Au weight in PCB}} \quad (2)$$

TABLE IV

SUMMARY OF THE NUMBER OF COMPONENTS FAILED AFTER RANDOM VIBRATION AND MECHANICAL SHOCK TESTS

	Flash Au Board			Thick Au board		
	As-built	After thermal aging for 30 days	After thermal aging for 56 days	As-built	After thermal aging for 30 days	After thermal aging for 56 days
QFN5	0/54	0/45	4/45*	3/54*	3/54*	3/53*
QFN6	6/54**	5/45**	5/45**	6/54**	5/54**	6/54**
TOPS	0/54	1/45	0/45	2/54	7/54***	2/54
FP I	24/36	26/30	20/30	All daisy chains had open solder joints after assembly		
FP II	27/36	25/30	19/30	All daisy chains had open solder joints after assembly		

Notes: * all failed components of QFN5 are in location AT30, which is near the mounting hole.

** all failed components of QFN6 are in location U18, which is near the mounting hole.

*** these seven failed components of TOPS are in one board. X-ray images show that there are very large voids on many solder joints on the TOPS component.

The number of components that failed after random vibration for 500 minutes and mechanical shock for 100 times is summarized in Table IV. The numerator in each cell refers to the number of failed daisy chains and the denominator refers to the total number of components in the reliability test.

After examining the locations of the failed QFN5 and QFN6 components, we found that all of the failed QFN5 components occurred at location AT30, and all of the failed QFN6 components were at location U18. AT30 is located at the lower left corner of the test vehicle shown in Fig. 1 and U18 is located at the upper left corner of the test vehicle. Both locations are near the mounting hole. This indicates that high strain during the board flexure in the drop and random vibration testing caused the failure of solder joints under these components. Excluding the components near the mounting holes, none of the QFN5 and QFN6 components failed in any of the test groups. Thus, we concluded that all QFN solder joints, which have Au content up to 5 wt%, are reliable, and thermal aging at 125 °C for up to 56 days does not cause significant degradation in reliability. Note that Cu from the QFN component lead is present to diffuse into the solder joints in this case.

After examining over 25 SEM images of failed solder joints for the QFN components, we found that the failure mode on flash Au boards is different from that on thick Au boards. The failure mode on flash Au boards was fracture in the Sn matrix at the bulk solder joint as shown in Fig. 4. The IMC near the component side is $(\text{Cu}, \text{Ni}, \text{Au})_6\text{Sn}_5$ and has 32 wt% Cu, 1 wt% Ni, 6 wt% Au, and 61 wt% Sn. The IMC near the board side is $(\text{Cu}, \text{Ni}, \text{Au})\text{Sn}$, which could be a mix of $(\text{Cu}, \text{Au})_6\text{Sn}_5$ and $(\text{Ni}, \text{Au})_3\text{Sn}_4$, and has 22 wt% Cu, 8 wt% Ni, 6 wt% Au, and 64 wt% Sn.

There were two failure modes of the QFN components on thick Au boards. The first was fracture in the Sn matrix at the bulk solder joint and at the IMC near the component side or

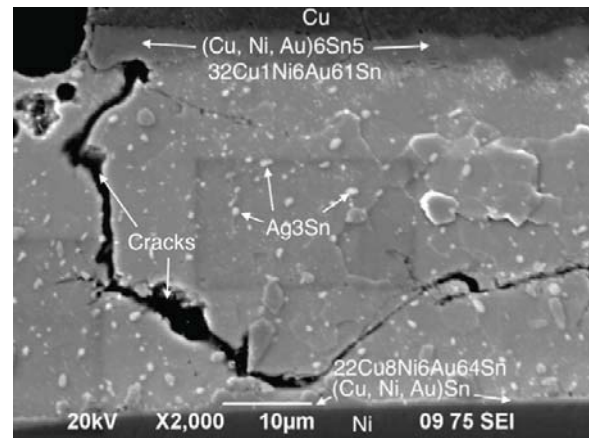


Fig. 4. Fracture in bulk solder of a QFN on a flash Au board, after thermal aging for 56 days.

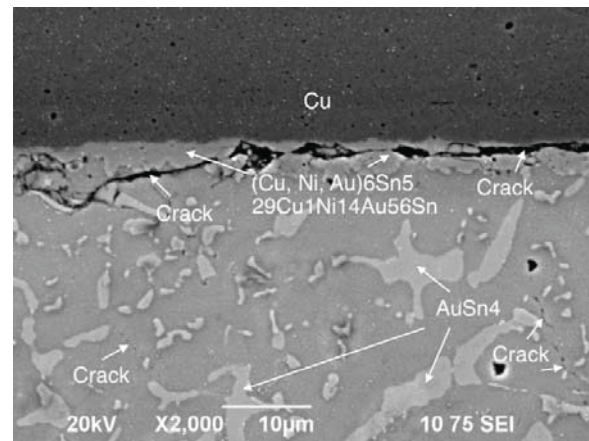


Fig. 5. Fracture in bulk solder joint and IMC near component side, a QFN on a thick Au board, as-built.

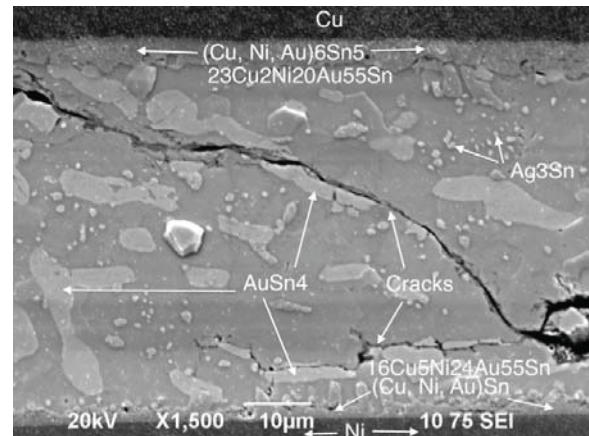


Fig. 6. Fracture in AuSn_4 IMC in the bulk solder, a QFN component on a thick Au board, after thermal aging for 56 days.

near the board side in the as-built samples. The second failure mode is fracture through the AuSn_4 IMC in the thermally aged samples. After thermal aging, smaller AuSn_4 IMCs combined and became larger AuSn_4 IMCs. Fig. 5 shows fracture in the bulk solder and at the IMC near the component side in an as-built sample, and Fig. 6 shows fracture in the AuSn_4 IMC.

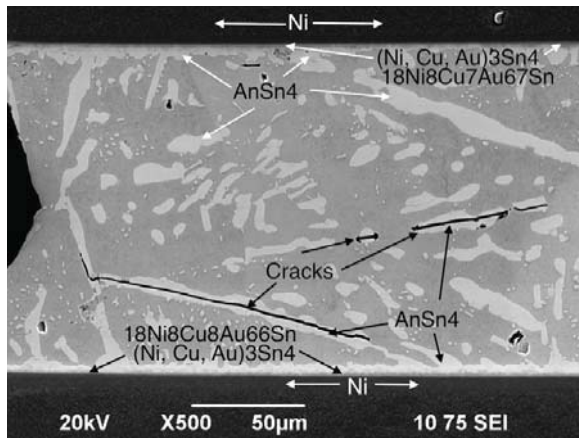


Fig. 7. Fracture in AuSn₄ IMC in the bulk solder, a TOPS component on a thick Au board, after thermal aging for 30 days.

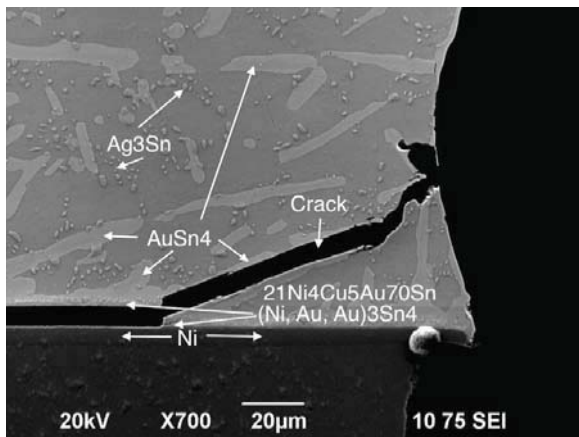


Fig. 8. Fracture in the IMC near the board side, a TOPS component on a thick Au board, after thermal aging for 30 days.

Fractures could begin at the middle of the bulk solder, the outside of the bulk solder, as well as the IMC interface near the board or the component. We can conclude that: 1) if the size of AuSn₄ IMC is small enough, the failure mode is fracture in the Sn matrix of the bulk solder when the solder joint is under high strain, and 2) if the size of AuSn₄ IMC is large enough, the failure mode is fracture through the AuSn₄ IMC for solder joints under mechanical reliability testing. After further examining the location of failed solder joints on both flash Au boards and on thick Au boards, we found that it was always the solder joints closest to the mounting hole that failed. It is clear that high strain leads to the failure of these solder joints.

For the TOPS components, it appears that the reliability of solder joints on the flash Au boards is better than that of solder joints on the thick Au boards since only one failed out of 144 components on the flash Au board while 11 components failed out of 162 components on the thick Au boards. Note that seven failed components were on the same thick Au board. The SEM images in Figs. 7 and 8 demonstrate that the failure mode is fracture in the AuSn₄ IMC in the bulk solder and in the IMC interface near the board side, respectively. In addition to a large amount of AuSn₄ IMC in the bulk solder joint contributing to

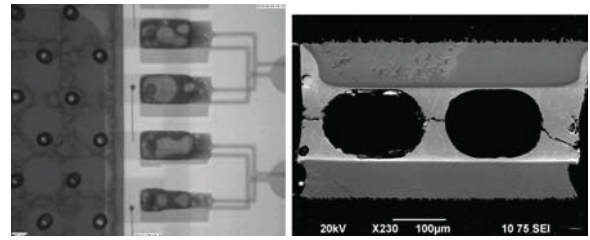


Fig. 9. X-ray image and an SEM image showing voids in the solder joints of a TOPS component on a thick Au board.

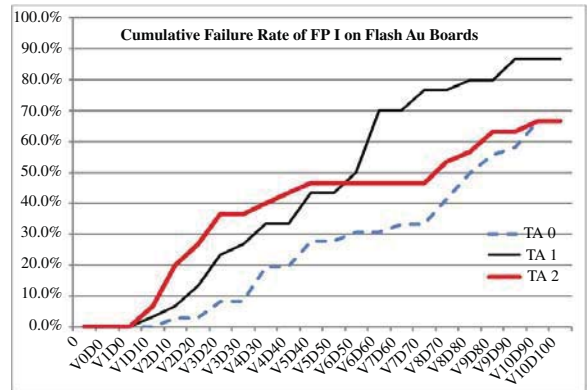


Fig. 10. Cumulative failure rate of FP I components on flash Au boards. TA0 represents as-built, TA1 represents thermal aging at 125 °C for 30 days, TA2 represents thermal aging at 125 °C for 56 days, and VID10 in the x-axis represents 1 cycle (or 50 mins) of random vibration and 10 drops.

the failure of solder joint, voiding is another factor. We noticed that there are large voids in solder joints on all failed TOPS components on the thick Au board, although not every failed joint had large voids. It will be interesting to investigate why the voids were specific to these parts and this gold content. An X-ray image and an SEM image in Fig. 9 clearly show the voids on one failed component.

Note that one significant difference between the IMC in QFN solder joints and the IMC in TOPS solder joints is that more Cu was dissolved into the solder joint from the Cu lead of the QFN component, while limited Cu was dissolved from the TOPS lead due to the Ni finish. The detailed microstructural analysis of these components will be published in the Journal of Electronic Materials [19]. We conclude that if Ni layers exist on both the board side and the component side, which limits the available Cu to dissolve into the solder joint, an Au content less than 3% in weight is acceptable for SnAgCu solder. From the results of the QFN components, we conclude that if Cu is available to dissolve in the solder joint, an Au content of less than 5% in weight is acceptable for SnAgCu lead-free solder.

For FP I and FP II components, all of the components on the thick Au boards failed (completely open or with very high resistance) immediately after assembly, while all components on the flash Au boards passed initial electrical test. About two-thirds of the components on the flash Au boards failed after the mechanical shock and random vibration testing. The cumulative failure rate of these 96 FP components on flash Au boards is shown in Figs. 10 and 11. It is clear that

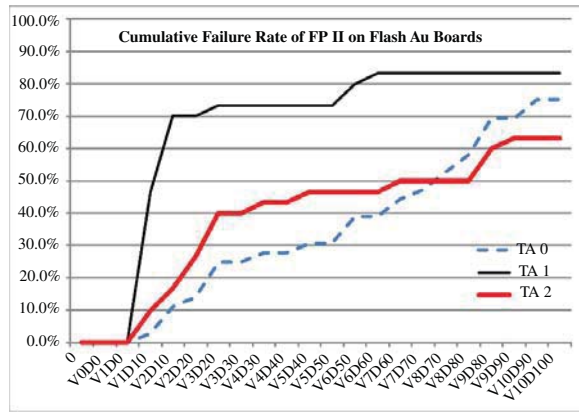


Fig. 11. Cumulative failure rate of FP II components on thick Au boards. TA0 represents as-built, TA1 represents thermal aging at 125 °C for 30 days, TA2 represents thermal aging at 125 °C for 56 days, and VID10 in the x-axis represents 1 cycle (or 50 mins) of random vibration and 10 drops.

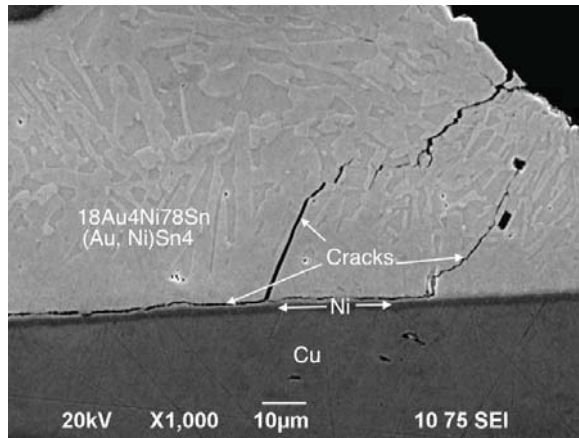


Fig. 12. SEM images of solder joints of an FP component on a flash Au board, after thermal aging for 56 days.

solder joints started to fail after 1 cycle (50 mins) of random vibration. It was observed that many FP components on the thick Au boards fell off the boards during the mechanical reliability tests. Thus, solder joints with an Au content over 10% are not acceptable.

Fig. 12 shows the microstructures of a typical solder joint of a FP component. The entire solder joint consists of (Au, Ni)Sn₄ IMC with around 18 wt% of Au, 4 wt% of Ni, and 78 wt% of Sn. The fracture is in (Au, Ni)Sn₄ IMC in the bulk solder near the board side. It is expected that the microstructures of the entire solder joint are AuSn₄ or (Au, Ni)Sn₄ IMC, if the Au content is close to 20% in atomic fraction. Note that there is a Ni layer in the FP component, preventing diffusion of copper into the joint.

IV. CONCLUSION

A comprehensive study has been conducted investigating the effect of Au content on the reliability of lead-free solder joint. The results show that SAC305 solder joints with over 10 wt% Au are unacceptable. If Cu is available to dissolve into the solder joint, then an Au content under 5 wt% will not significantly degrade the reliability of the solder joint. When

Ni layers are present on both the board and component sides of the interface, limiting the ability of Cu to dissolve into the solder joint, an Au content under 3 wt% is acceptable. Additional findings confirmed the danger of placing parts near high-stress areas and that a high level of voiding reduced reliability.

When the Au content in a solder joint is less than 3 wt%, AuSn₄ IMCs are small and will not play a significant role. The failure mechanism of such a solder joint is fracture within the Sn matrix when the joint is subjected to a very high stress level. If the Au content is high or large AuSn₄ IMCs are present in a solder joint, the failure mechanism is fractures through the AuSn₄ IMCs. Fractures through the AuSn₄ IMCs were found in the bulk solder and/or near the solder–metallization interface.

ACKNOWLEDGMENT

J. Pan is grateful to Agilent Technologies, Santa Clara, CA, for funding this project during his sabbatical leave. The authors would like to thank B. Jones of Agilent for technical support and advice on reliability testing conditions, D. Gibbons and J. Bishop of Agilent Technologies, Santa Rosa, CA, for reliability testing setup, S. Sethuraman of Jabil, San Jose, CA, for assembling the boards, and R. Savage at California Polytechnic State University, San Luis Obispo, CA, for assistance in scanning electron microscope analysis.

REFERENCES

- [1] G. Humpston and D. M. Jacobson, *Principles of Soldering*. Materials Park, OH: ASM, 2004, p. 82.
- [2] W. G. Bader, "Dissolution and formation of intermetallic in the soldering process," in *Proc. Symp. Phys. Metall. Metal Join.*, 1980, pp. 257–268.
- [3] W. G. Bader, "Dissolution of Au, Ag, Pd, Pt, Cu, and Ni in a molten tin-lead solder," *Weld. J.*, vol. 48, no. 12, pp. 551–557, 1969.
- [4] C. E. Ho, L. C. Shiau, and C. R. Kao, "Inhibiting the formation of (Au_{1-x}Ni_x)Sn₄ and reducing the consumption of Ni metallization in solder joints," *J. Electron. Mater.*, vol. 31, no. 11, pp. 1264–1269, 2002.
- [5] M. O. Alam, Y. C. Chan, and K. N. Tu, "Elimination of Au-embrittlement in solder joints on Au/Ni metallization," *J. Mater. Res.*, vol. 19, no. 5, pp. 1303–1306, 2005.
- [6] M. O. Alam, B. Y. Wu, Y. C. Chan, and L. Rufer, "Reliability of BGA solder joints on the Au/Ni/Cu bond pad-effect of thicknesses of Au and Ni layer," *IEEE Trans. Dev. Mater. Rel.*, vol. 6, no. 3, pp. 421–428, Sep. 2006.
- [7] J. Glazer, P. A. Kramer, and J. W. Morris, Jr., "Effect of gold on the reliability of fine pitch surface mount solder joints," *Circuit World*, vol. 18, no. 4, pp. 41–47, 1993.
- [8] C. W. Chang, C. E. Ho, S. C. Yang, and C. R. Kao, "Kinetics of AuSn₄ migration in lead-free solders," *J. Electron. Mater.*, vol. 35, no. 11, pp. 1948–1954, 2006.
- [9] L. C. Shiau, C. E. Ho, and C. R. Kao, "Reactions between Sn-Ag-Cu lead-free solders and the Au/Ni surface finish in advanced electronic packages," *Solder. Surf. Mount Technol.*, vol. 14, no. 3, pp. 25–29, 2002.
- [10] D. S. Steinberg, *Vibration Analysis for Electronic Equipment*, 2nd ed. New York: Wiley, 1988.
- [11] *Vibration Data Collection: A Road Worth Traveling?* L.A.B. Equipment, Inc., Itasca, IL, 2006.
- [12] *Method 514.6, U.S. Department of Defense*, Standard MIL-STD-810G, Oct. 2008, pp. 288–289.
- [13] J. H. Lau, N. Hoo, R. Horsley, J. Smetana, D. Shangguan, D. Dauksner, D. Love, I. Menis, and B. Sullivan, "Reliability testing and data analysis of lead-free solder joints for high-density packages," *Solder. Surf. Mount Technol.*, vol. 16, no. 2, pp. 46–68, 2004.
- [14] M. Farooq, L. Goldmann, G. Martin, C. Goldsmith, and C. Bergeron, "Thermo-mechanical fatigue reliability of Pb-free ceramic ball grid arrays: Experimental data and lifetime prediction modeling," in *Proc. 53rd IEEE Electron. Comp. Technol. Conf.*, New Orleans, LA, May 2003, pp. 827–831.

- [15] J. C. Suhling, H. S. Gale, R. W. Johnson, M. N. Islam, T. Shete, P. Lall, M. J. Bozack, J. L. Evans, P. Seto, T. Gupta, and J. R. Thompson, "Thermal cycling reliability of lead-free chip resistor solder joints," *Solder. Surf. Mount Technol.*, vol. 16, no. 2, pp. 77–87, 2004.
- [16] *Board Level Drop Test Method of Components for Handheld Electronic Products*, JEDEC Standard JESD22-B111, 2003.
- [17] *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*, Standard IPC-9701, 2002.
- [18] G. Henshall, J. Bath, S. Sethuraman, D. Geiger, A. Syed, M. J. Lee, K. Newman, L. Hu, D. H. Kim, W. Xie, W. Eagar, and J. Waldvogel, "Comparison of thermal fatigue performance of SAC105 (Sn-1.0Ag-0.5Cu), Sn-3.5Ag, and SAC305 (Sn-3.0Ag-0.5Cu) BGA components with SAC305 solder paste," in *Proc. IPC APEX*, 2009, pp. 1–11.
- [19] M. Powers, J. Pan, J. Silk, and P. Hyland, "Effect of gold content on the microstructural evolution of SAC305 solder joints under Isothermal Aging," *J. Electron. Mater.*, Mar. 2011.



Jianbiao John Pan (M'03–SM'07) received the B.E. degree in mechatronics from Xidian University, Xian, China, in 1990, the M.S. degree in manufacturing engineering from Tsinghua University, Beijing, China, in 1996, and the Ph.D. degree in industrial engineering from Lehigh University, Bethlehem, PA, in 2000.

He is an Associate Professor from the Department of Industrial and Manufacturing Engineering, California Polytechnic State University (Cal Poly), San Luis Obispo. Prior to joining Cal Poly, he

was with the Optoelectronics Center of Lucent Technologies, Breinigsville, PA/Agere Systems Inc., Allentown, PA, as a Technical Staff Member. His current research interests include environmentally benign microelectronics packaging and reliability including lead-free soldering and light-emitting diode packaging. His teaching interests include electronics manufacturing, microelectronics and electronic packaging, statistical data analysis, design and analysis of experiment, quality engineering, and reliability engineering.

Dr. Pan is a recipient of the M. Eugene Merchant Outstanding Young Manufacturing Engineer Award in 2004 from the Society of Manufacturing Engineers. He is the first-place winner of the Association Connecting Electronics Industries. Worldwide Academic Poster Competition in 2009. He is a Highly Commended Winner of the Emerald Literati Network Award for Excellence in 2007. He is a Fellow of the International Microelectronics and Packaging Society.



Julie Silk is the Environmental Compliance Technical Program Manager for the Electronic Measurements Group of Agilent Technologies, Santa Rosa, CA. She has over 25 years of experience with printed circuit assembly processes, quality, reliability, design for manufacturability, and supplier development. She is currently engaged in the restriction of hazardous substances transition for Agilent, focusing on maintaining or improving the quality and reliability of Agilent products.



Michael T. Powers received the B.S. and M.S. degrees in Materials Science and Engineering from the University of California, Berkeley, in 1989 and 1992, respectively.

He is currently a Materials Scientist in the Electronic Measurements Group of Agilent Technologies, Santa Rosa, CA, where he has been working for the past 20 years. His technological expertise is in the field of joining process technology, including glass-to-metal sealing, active metal brazing, reactive joining, and lead-free soldering. He holds eight

U.S. patents, with in the areas of chemical engineering and high-frequency connector design. He has published a number of technical papers on joining of advanced engineering materials and materials characterization, and served as an editor for the *CRC Materials Processing Handbook* (CRC Press, 2007), and various conference proceedings. In 1995, he codeveloped a non ozone depleting solvent chemistry to replace CFC-113 for critical cleaning of components used in the electronics industry. He is a Lecturer in the Department of Chemical Engineering and Materials Science at the University of California, Davis, where he teaches a senior-level capstone project course called Materials Design Project (Engineering Materials Science 188).

Mr. Powers received the U.S. Department of Energy Pollution Prevention Award in 1996 and the Excellence in Technology Transfer Award from the U.S. Federal Laboratory Consortium in 1997. He is a member of the American Welding Society, the Minerals, Metals and Materials Society and a Fellow of the American Society for Metals International.



Patrick Hyland is pursuing a M.S. degree in materials engineering at California Polytechnic State University (Cal Poly), San Luis Obispo.

He has been the Principal Scanning Electron Microscope Operator for his department, while at Cal Poly. His work experience includes an internship at Washington State University, Pullman. His current research interests include semiconductor processing, metallurgy, applied statistics, and electronics.