A Self-Oscillating Parallel Audio Amplifier

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Abstract—A design for a parallel audio amplifier attempts to improve on existing amplifier topologies by combining a high fidelity linear analog amplifier in parallel with a high efficiency Class-D switching amplifier. A working model demonstrates self-oscillation according to theory but low efficiency results prevent the amplifier from becoming a good alternative in low-power applications.

Index Terms—audio amplifier, Class-D, switching amplifiers, parallel amplifier, sustainability

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Breadboard prototype.  

Breadboard prototype.  

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I. Design Requirements

Build a high-efficiency, high-fidelity headphone amplifier suitable for use in small, portable electronics.

II. Project Specifications

Design a 1 watt audio amplifier with > 80% efficiency and < 0.5% THD using a self-oscillating parallel amplifier configuration. The design should take a line level musical input (such as an mp3 or CD player) and output the signal to a small speaker. The finished product should run off of a 12V 1350mAh battery for five or more hours.

III. Introduction, Project Goals, Motivation, Context and Justification

The growing field of personal electronics now includes many products with previously unseen functionality. Users often expect their devices to simultaneously play music, surf the Internet, send text messages, and run a myriad of software applications. This puts significant power demands on physically shrinking devices and escalating competition in the marketplace puts increasing importance on efficient, high-performance designs.

Demand for high-efficiency audio amplifiers rises with the increasing ubiquity of small, portable electronics. In general, efficiency only increases at the expense of fidelity. Despite the high fidelity characteristics of Class-A and Class-AB amplifiers, their high static power consumption prevents their widespread use outside of large, cumbersome amplifiers with significant power dissipation capabilities [1]. Alternative designs such as Class-D amplifiers combat low efficiencies using switching and pulse width modulation techniques. While Class-D amplifiers improve efficiency, high-frequency components from the switching action add distortion at the output [1]. The designs proposed in [1-5] attempt to combine AB and D amplifiers in novel ways in order to retain the high efficiencies of Class-D amplifiers and the high fidelity of Class AB amplifiers. These combination amplifiers not only increase the functionality of audio playback in electronic devices but also extend their lifespan, reducing electronic waste and decreasing the total power consumption of the user.

A successful parallel amplifier configuration uses an AB section as a high-fidelity voltage-controlled voltage source. The AB amplifier subsequently controls a high-efficiency switching amplifier that provides the majority of the output current. The final design retains the high fidelity of the AB amplifier and the high efficiency of the switching network. The following paper proposes to design, construct, and test a basic version of a parallel linear/switching amplifier using a current monitoring approach. Section IV analyzes the overall scope of the project using a set of criteria established by the Accreditation Board for Engineering and Technology (ABET). Section V gives insight into both the research and planning process. Section VI summarizes different classes of amplifiers and introduces techniques to combine them in both series and parallel combinations. Section VII gives an in-depth description of a current-monitoring parallel amplifier, the self-oscillating switching network, and some derivations of equations defining amplifier performance. Section VIII describes each subsystem in more detail and describes component requirements. Section IX gives a cost breakdown for the project. Section X describes simulations performed in LTSpice and Section XI gives details related to the construction. Section XIII gives efficiency results and XIV gives distortion results. Finally, Section XV summarizes the project and provides suggestions for improved designs.

IV. ABET Analysis

The following section outlines the economic, environmental, sustainability, manufacturability, ethical, health and safety, social, and political considerations applicable to the parallel amplifier design.

A. Economic

High-efficiency designs increase the functionality of personal electronics. Modern devices like the iPhone typically need recharging after several hours of use. Users increasingly rely on these devices for both social and professional needs and make purchasing decisions based on expected battery life. Additionally, users with discerning taste often take issue with the audio quality of their phones, mp3 players, and video playback devices. A product capable of delivering high quality audio with low power demands represents a major boon to companies wishing to profit in a lucrative but highly competitive market.

While developments in battery technology increase charge capacity, exotic battery designs and involved charging schemes add to design complexity, development time, and the total cost of a product. While the emphasis on small, high storage batteries probably will not subside, low power demands give additional flexibility to designers and offer lower cost alternatives than may currently exist.

B. Environmental

Electronic components damage the environment during both manufacture and disposal. Without proper processing, the introduction of harmful substances such as lead and mercury into the environment represents a major hazard. Electronic waste poses a significant health risk for ecosystems near disposal centers from chemicals leaching into soil and water supplies. Additionally, easily recyclable materials like aluminum and copper often sit in landfills unused. These issues apply specifically to batteries, which lose their ability to store energy over time. Improper disposal may release lead, acid, and heavy metals into the environment. Lowering energy requirements naturally extends battery lifespan and increases the usability of a product. This leads to a dramatic decrease in environmental damage by minimizing consumption and reducing the amount of waste entering the ecosystem.

C. Sustainability

Modern phones, computers, and media players utilize incredibly powerful technologies. Single devices serving multiple purposes now replace multiple devices each serving a
The utility of electronic devices comes from not only raw processing power but usability and flexibility as well. While this decreases the total volume of devices requiring manufacturing, maintenance, and disposal, it also introduces many subtle requirements regarding design. Again, the battery systems of small electronics become a bottleneck. Increasing the life span of an electronic device relies on decreasing its total power consumption while simultaneously improving or maintaining its total value to the user.

The power consumption of a device extends to more than just the internal efficiency. Batteries rely on inefficient DC power supplies. These rely in turn on inefficient power generation and transmission facilities. Increasing efficiency not only increases the lifespan of products but also reduces unintended losses and puts fewer requirements on generation capacity.

While somewhat cynical, consumer societies show that individuals often concern themselves with immediate experience rather than the long-term consequences of their actions. A high fidelity, high efficiency amplifier combines both usability and sustainability into a single design. Although small audio amplifiers may seem trivial, a high efficiency high fidelity product still represents a step towards a more sustainable society. Engineers tasked with energy efficient design will influence their colleagues, and products designed with sustainability in mind will likely be marketed accordingly. This will influence both spending and usage habits for a society increasingly defined by advertising and material culture.

D. Manufacturability

The basic design of a parallel amplifier should not require any exotic components or outlandish manufacturing techniques. In fact, the parallel amplifier design proposed in [1] lend itself to the CMOS implementation process. A parallel amplifier relies on using existing circuit components to create a new amplifier architecture.

A successful parallel amplifier probably increases design complexity compared to an AB amplifier alone. The requirement of additional, carefully chosen hardware represents a drawback (see Sections VII and VIII). Parallel amplifiers use more physical space than class AB alone, and often require large-value physical inductors for output filtering.

E. Ethical

The IEEE Code of Ethics explicitly states that members must [6]:

1) Accept responsibility in making decisions consistent with the safety, health and welfare of the public, and to disclose promptly factors that might endanger the public or the environment.
2) Improve the understanding of technology, its appropriate application, and potential consequences.
3) Treat fairly all persons regardless of such factors as race, religion, gender, disability, age, or national origin.

These items directly relate to energy efficient design. The safety, health, and welfare of both the public and the environment depend on reducing consumption and increasing the utility of modern personal electronics. The continued viability of both the human race and the earth as a whole depends on rethinking energy demands at every level of consumption. While the odds of an audio amplifier bringing dramatic change to the industry are low, increasing attention to energy use and environmentally sound practices will nevertheless help contribute to creating a climate of environmental and ethical sustainability.

Item 3) demands socially responsible practices from designers. Unfortunately, current manufacturing and disposal practices often involve overseas facilities staffed by underpaid, heavily exploited workers. The high profitability of fashionable gadgets will continue to negate both social and political movements towards reform. The ethical treatment of the world’s citizens thus requires a framework that stresses the long-term consequences of modern devices. Sustainable design reduces the burden impressed on the underprivileged by consumer societies and helps progress the issues of equality and cooperation.

F. Health and Safety

Electronic waste poses a significant threat to the health and safety of the surrounding community. With many disposal sites located in underdeveloped countries, E-waste is an incredible risk to societies that frequently lack even basic health and sanitation services. Undeniably, efforts to extend product lifespan result in more utility and less waste.

G. Social and Political

While developed countries work to decrease their impact on the environment, they regularly decide to simply send their undesirable materials to other, less developed societies. This distances consumers from the consequences of their actions. While the negative impacts of consumption may alleviate stress on the local environment, the total cost to society remains the same. Furthermore, removing the direct effects of a modern lifestyle helps maintain archaic political power structures that stress profit over morality and competition over cooperation. The socially responsible global economy thus depends on active representation for all the world’s citizens.

Inefficient designs serve to maintain dependence on harmful energy production facilities and the companies that maintain them. Independence from established hierarchies naturally results in greater social, political and economic mobility. Necessary political and social change in the 21st century depends on reforming current energy dependencies. Efficient and usable electronics reduce the burden on developing countries by decreasing the need for cheap labor and diminishing the amount of damage done to their environment during both the manufacturing, use, and disposal cycles.

V. Literature Search, Proposal and Timeline

Fig. 37 shows the project timeline from start to finish (see Appendix). The design requirements for the parallel amplifier arose while doing research for a senior project needed for graduation from Cal Poly, San Luis Obispo’s Electrical
Engineering Department. Initial research focused on finding a project that combined electronic design, music, and a physical deliverable in a new or interesting way. Investigation at the library and on the internet quickly led to designs laid out in [1], [3] and [5] using both class AB and class D amplifiers in tandem. A project proposal submitted to Dr. David Braun on January 3rd, 2011 quickly led to two tentative timelines (see Figs. 38 and 39). Research began in earnest later that same month.

The research phase determined most of the specific criteria and direction for the project. The "Class K" amplifier in [3] presented the idea of a parallel amplifier using current monitoring but didn’t provide enough information to guide the project. The "Class-K*" presented in [1] was elegant but too complex for an undergraduate design project. Somewhat serendipitously, [2] and [4] by Ronan van der Zee explained self-oscillating parallel amplifiers in great detail, including considerations relating to intended switching frequency, bandwidth, impedance, power dissipation, and the measurement for both efficiency and distortion (see Section VII). Although the paper didn’t provide any specific schematics or circuit designs, [2] proved to be crucial towards explaining many of the subtleties of the amplifier.

Research ended in mid-February and led to the design stage where a circuit schematic developed slowly using LTSpice. Proper operation of the amplifier requires balancing many different criteria (such as current sensing and power handling), and inaccurate component values caused unwanted oscillations that stalled the computer simulations without providing meaningful data. Several Microsoft Excel programs plotted the circuit operation visually and led to more accurate component choices. Circuit simulation continued and the schematic slowly formed into its final incarnation. See Section X for simulation results.

Research into component choice began in early March (see Section VIII). Components sourced on the internet were compared for performance and price. The top two or three options were purchased in order to have some freedom of choice while constructing the circuit. Conflicting engagements during the second half of March slowed progress on the amplifier, although documentation performed from March 22-27 helped summarize previous steps and prepare for the construction and testing phases.

The physical construction of the amplifier circuit presented the most challenging aspect of the project. The original project timeline grossly underestimated the time needed for construction. Putting together a working model took the better part of both April and May (see Section XI). The two last weeks of May saw the simultaneous completion of the physical circuit, testing, and final documentation. The project reached completion upon presenting it at the Cal Poly Electrical Engineering Department’s Spring 2011 Senior Project Exhibition and subsequently submitting this paper to the Cal Poly Library.

VI. SERIES AND PARALLEL AMPLIFIERS

Different classes of amplifiers have their own distinct advantages and disadvantages regarding efficiency, fidelity, and design complexity. Series and parallel combinations use different classes in tandem to improve performance.

The following section goes over the main classes of audio amplifiers, different approaches taken to combine these classes in novel ways, and attempts to provide insight into the eventual choice of a self-oscillating amplifier using the current monitoring approach.

While they both have their own distinct advantages and disadvantages, a parallel amplifier using current monitoring represents the best tradeoff for simplicity, expense, design time, and the overall scope of this project.

A. Class A and Class AB

Fig. 1 shows a typical class A amplifier. Class A amplifiers have high fidelity but low efficiencies - often lower than 25% [10]. The low efficiency results from the amplifier conducting during all cycles of output, including zero output. This quiescent conduction contributes nothing to output power and only serves to bias the transistor. A simple modification, called class AB, uses two transistors in a push-pull stage to reduce quiescent current (Fig. 2). Only one transistor conducts at a time, preventing conduction during low-output and increasing efficiency. The push-pull stage lowers the fidelity of the amplifier by introducing unpleasant crossover distortion resulting from the transistors turning on and off near zero voltage crossings. Crossover distortion heavily degrades sound quality, even in small amounts [2]. The maximum theoretical efficiency of a class AB stage is 78.5% for a full power sine wave. This number decreases greatly when amplifying most music, especially quiet music played at low volume [2], [10].
B. Class D

Class D amplifiers like that in Fig. 3 use techniques such as pulse-width modulation, pulse-density modulation, or $\Delta\Sigma$ modulation to convert an analog input signal to a series of pulses [10]. Class D amplifiers have a theoretical efficiency of 100% and practical efficiencies often above 90% [2]. The high efficiency of class D amplifiers comes from the lack of resistive components delivering power to the load. The load current flows through low-resistance switches into an output filter usually consisting of inductors and capacitors. These components ideally dissipate no power, although in practice they have a low amount of inherent resistance. The switching network converts the input to a series of pulses with lengths proportional to the magnitude of the input. The output switches take turns sinking and sourcing current in the shape of a pulse train. The switching action adds high-frequency spectral components and requires a low-pass filter at the output to recover the original signal. The drawbacks for class D amplifiers include lowered fidelity from residual high-frequency components, added complexity from additional circuitry, and the need for complex output filtering networks [2]. Class D amplifiers require careful design to reduce switching problems such as shoot-through, overshoot, and poor tracking between switching times [7].

C. Series Amplifiers

Series amplifiers use linear and switching amplifiers in a series connection. The most common design uses a switching amplifier to generate the source voltage of the linear section [2]. Most of the quiescent power dissipation of a Class AB amplifier results from the voltage drop across the transistor. Lowering the source voltage during periods of low output reduces the voltage drop across the amplifying transistor and decreases power consumption. A class D used to generate the supply voltage lets the circuit dynamically respond to output power, only increasing the source voltage when necessary (see Fig. 4). Since all transistors carry all the output current, chip sizing becomes an issue [2]. In addition, timing requirements add additional complexity and require some sort of voltage monitoring across the load.

D. Parallel Amplifiers

Many different competing parallel amplifier designs exist [1-5]. Fig 5 shows the simplest and most straightforward design. A class A or class AB amplifies the input signal and controls the output voltage. It also controls the operation of the switching section. Efficiency improves by using the switching amplifier to provide the majority of power to the load. The analog section still uses some quiescent power. The switching control section monitors the small current output from the AB amplifier and directs the switches to sink or source load current appropriately.

The current monitoring required in Fig. 5 presents one drawback. Accurate current monitoring using a floating load presents complex challenges, especially given small voltages at high frequencies [1]. Other designs use more exotic techniques such as current dumping [1]. Fig. 6 uses a technique called fast switching charge dumping. As usual, a highly linear class AB section drives a PWM class D section. Major modifi-
cations include a fast switching charge-dump circuit at the output to the class AB. This quickly sources or sinks current and increases both the accuracy of switching and efficiency. Drawbacks include increased complexity, especially since the charge-dump technique requires careful design [7-9].

VII. CIRCUIT DESCRIPTION

Fig. 7 shows the block diagram of the proposed amplifier. A highly linear class AB amplifier controls output voltage while the efficient class D provides current. The AB amplifier outputs an audio signal to the current sensing device A. The current sensor monitors the output current and performs the switching logic for the MOSFETs. In this technique, one of either SW$_1$ or SW$_2$ conducts at any given time. The Class-D section supplies most of the power to the load but adds distortion from the switching action in the form of ripple current. The analog amplifier counteracts this distortion and lowers the overall total harmonic distortion (THD) by either providing or absorbing extraneous current. The inductor L$_1$ integrates $\pm V_s$ and limits the rate of current flowing through the speaker. This inductor performs a similar function to the output filters in more traditional Class D amplifiers but with simpler implementation. Shown later, the main concerns for the inductor are slew rate and the desired operating frequency of the switching section.

A. Switching Frequency and Bandwidth

The chosen parallel amplifier self-oscillates at a variable frequency dependent on component choices, output power, and the instantaneous value of output voltage. As an example, consider the positive portion of a sine wave. SW$_1$ opens and dumps the required current through both L$_1$ and the speaker. The inductor integrates the source voltage and keeps the current from spiking instantaneously. As the current through L$_1$ increases, the current required of AB decreases. Eventually, $I_{L1}$ increases above the value required by the load and AB begins to absorb current. The current sensing device A monitors the current up to the threshold current $I_{thr}$, at which point it switches off SW$_1$ and switches on SW$_2$. Figs. 8 and 9 show typical current profiles.

The instantaneous switching frequency fluctuates and depends on the choice of threshold current $I_{thr}$, inductor value L$_1$, source voltage $V_s$, load impedance $R_{LS}$, instantaneous output voltage, and intended bandwidth of the amplifier. Eqn. 1 gives the relation for the instantaneous switching frequency.

$$f_{switch} = \frac{V_s^2 - (V_o + \frac{L_1}{R_{LS}} \cdot \frac{dV_o}{dt})^2}{4I_{thr}L_1V_s}$$ (1)

The switching frequency depends on the instantaneous output voltage of the signal and fluctuates accordingly. Maximum frequency occurs near zero output voltage while minimum frequency occurs near the peak. Fig. 10 shows an example of how switching frequency fluctuates for different output voltages.

The numerator of Eqn. 1 shows a theoretical circumstance with zero switching frequency. This defines the power bandwidth of the switches. The current through inductor L$_1$ cannot spike instantaneously, limiting the amount of power available from the switches for high frequency signals. For
Fig. 10. Plot of switching frequency (solid) for a 1kHz sine wave output (dotted) using Eqn. 1 with \(L_1 = 0.3\, \text{mH}\) and \(I_{\text{thr}} = 35\, \text{mA}\).

Fig. 11. Current profiles through load, inductor, and analog section. The AB amplifier supplies part of the output current, lowering efficiency [2].

Fig. 12. Plot of switching frequency (solid) for a 5kHz sine wave output (dotted) using Eqn. 1 with \(L_1 = 0.3\, \text{mH}\) and \(I_{\text{thr}} = 35\, \text{mA}\). At \(f_{\text{switch}} = 0\), the AB amplifier must supply part of the output current

\[
V_o = V_p \sin(2\pi ft) \quad \text{and} \quad \frac{dV_o}{dt} = 2\pi V_p f \cos(2\pi ft),
\]

Eqn. 2 gives the power bandwidth of the switching section [2]

\[
BW = \frac{R_{LS}}{2\pi L_1} \sqrt{\frac{1}{\left(\frac{V_p}{f}\right)^2}} - 1 \quad (2)
\]

At frequencies above the power bandwidth the switches cannot supply enough current through the inductor and force the AB amplifier to provide the remaining power. This lowers efficiency but otherwise does not affect amplifier fidelity. Figs. 11 and 12 show switching frequencies and current profiles when the switches cannot provide all the required output power.

Fig. 13 shows an example Microsoft Excel program used to calculate various circuit parameters used to generate the graphs in Figs. 10 and 12 using Eqns. 1 and 2.

**B. Impedance Considerations**

Fig. 14 shows the impedance \(Z_{o,AB}\) of the amplifier and \(Z_{LS}\) speaker. \(R_o\) is the DC output resistance of AB, \(L_0\) is the output inductance of AB, \(R_{LS}\) is the DC resistance of the speaker, and \(C_{LS}\) is the parallel capacitance of the speaker. Fig. 15 shows the schematic at high frequency. \(L_0\) dominates the AB output resistance \(R_o\) [2]. The voltage source \(V_{\text{switch}}\) is the node between \(SW_1\) and \(SW_2\).

Eqn. 3 gives the admittance model for Fig. 15.

\[
\begin{align*}
\frac{1}{Y} &= \frac{1}{R_{LS}} + \frac{1}{j2\pi f C_{LS}} + \frac{1}{R_o} \\
\frac{1}{Y} &= \frac{1}{j2\pi f L_0} + \frac{1}{R_o} \\
\end{align*}
\]
Fig. 15. Impedance model of amplifier at switching frequency [2].

\[ Y = \frac{1}{sL_1} \cdot \frac{1}{1 + \left( \frac{L_1}{L_o} \right) + s \frac{L_0}{R_{LS}} + s^2L_0C_{LS}} \]  

(3)

Ideally, Eqn. 3 simplifies to \( Y = \frac{1}{sL_1} \cdot \frac{1}{1 + \frac{L_1}{L_o} + s \frac{L_0}{R_{LS}}} \). This makes the current \( I_{AB} \) totally dependent on the choice of \( L_1 \), resulting in the well-behaved oscillation of Fig. 8. Fig. 16 gives a potential simplification. Putting an additional coil \( L_2 \) in series with the speaker gives the transfer function

\[ Y = \frac{1}{sL_1} \cdot \frac{1 + s \frac{L_2}{R_{LS}} + s^2L_2C_{LS}}{1 + s \frac{L_0 + L_2}{R_{LS}} + s^2(L_0 + L_2)C_{LS}} \]  

(4)

Imposing the condition \( L_2 >> L_0 \) makes the numerator and denominator of the second term cancel and simplifies the overall admittance to Eqn. 5.

\[ Y \approx \frac{1}{sL_1} \]  

(5)

In practice, the extra inductance required for \( L_2 \) can come from the inherent series inductance of the speaker.

C. Power Dissipation

The four main sources of power dissipation in the amplifier consist of the quiescent power of the AB amplifier \( P_{Q(AB)} \), the switching losses in the D section \( P_{Q(D)} \), the power dissipated in the current sensing network \( P_{sensing} \), and the extra power dissipated because of the inductor ripple [2].

\[ P_Q = P_{Q(AB)} + P_{Q(D)} + P_{sensing} + \frac{1}{2} V_s I_{thr} \]  

(6)

The quiescent power of the AB amplifier depends on the design used. While low-power AB amplifiers exist, lower AB quiescent power tends to conflict with demands for low output impedance [2]. The power demands of D consist mainly of the switching losses, conduction losses, and capacitive losses of the switches [2], [7]. Low power dissipation in the switches requires accurate timing, fast response time, and low on resistance \( R_{ds(on)} \). The power dissipated in the current sensing network depends on the quiescent power of both the instrumentation amplifier and the comparator. This is largely independent of the power delivered to the speaker. Consequently, the power dissipated in the sensing network could potentially lower efficiency in low power applications. Finally, the power dissipation from the current ripple is largely variable depending on \( I_{thr} \). Low values of \( I_{thr} \) increase switching frequency and decrease the extra power dissipated from the current ripple.

VIII. CIRCUIT DESIGN AND COMPONENT CHOICE

Fig. 17 shows the entire circuit. Fig. 40 in the Appendix shows a larger version. The following section outlines both the design of each section and the considerations given to specific components used.

A. Current Sensing Network

Most of the circuit complexity arises from the current sensing demands. The current sensing network must distinguish between \( \pm I_{thr} \) coming from AB and accurately control the MOSFET switches, all at low-to-medium frequencies (between 0 and 100kHz). The design tried to balance the conflicting demands for high efficiency and accurate switching performance. With the threshold current \( I_{thr} = 20mA \) the circuit responds with a maximum 120kHz switching frequency a 1.7kHz power bandwidth. Although high frequency signals decrease the efficiency of the amplifier, they do not have a significant presence in the audio spectrum of most music. The extra power demanded of the AB amplifier (and subsequent efficiency loss) probably does not warrant increasing the power bandwidth of the switches. A lower threshold current would increase both bandwidth and efficiency but put higher demands on the switching network. With \( I_{thr} = 20mA \), the switching network must detect a \( \pm 2mV \) voltage drop across \( R_{sense} \). A lower value of \( I_{thr} \) would thus require additional (and possibly unreasonable) accuracy from the current sensing network.
An instrumentation amplifier directly senses the voltage across the 0.1Ω current sensing resistor \( R_{\text{sense}} \) and monitors for the required ±2mV shift. \( R_{\text{sense}} \) does not dissipate much power because of the relatively small size of the oscillating threshold current compared to the load current. Larger values of \( R_{\text{sense}} \) would improve the accuracy of the current measuring but also increase the output impedance of the AB amplifier, lowering damping factor, decreasing available power to the load, and increasing distortion from the switching section. The small voltage shift requires high gain-bandwidth product, small offset voltage, high common-mode rejection ratio, and high input impedance from the instrumentation amplifier. A Texas-Instruments INA111 instrumentation amplifier has 20MHz GBW, 100µV offset voltage, 90dB CMRR, and \( 10^{12} \)Ω input impedance. A single external resistor \( R_G \) sets the gain anywhere between 1 and 1000 using the gain equation \( G = 1 + \frac{50k\Omega}{R_G} \). The use of only one resistor to set the gain represents a major advantage over other differential amplifiers that require four closely matched resistors for accurate performance. Additional connections for the INA111 include a voltage reference for the output tied to ground.

The voltage output from the instrumentation amplifier originally contained some unwanted transients and high frequency components (see Fig. 19). These could occur from power supply transients or reflections in the circuit. The INA111 datasheet [12] suggests the low-pass filter in Fig. 18. Eqn. 7 shows the calculation for the -3dB cutoff frequency.

\[
f_{-3dB} = \frac{1}{4\pi R_1(C_3 + C_2)}
\]  

The differential filter requires \( R_1 = R_2 \) and \( C_1 = C_2 \). Mismatches in \( C_1 \) and \( C_2 \) (either from tolerance or stray capacitance) lower the common-mode rejection of the filter. The differential input capacitor \( C_3 \) at a value much larger than \( C_1 \) and \( C_2 \) mitigates the effect of mismatch and preserves CMR [12]. Using \( C_1 = C_2 = 22pF \), \( C_3 = 240pF \), and \( R_1 = R_2 = 1.8k\Omega \) gives the cutoff frequency \( f_{-3dB} = 176kHz \). Fig. 20 shows the effect of the low-pass filter on the output of the instrumentation amplifier.

The output from the instrumentation amplifier feeds into a hysteretic comparator. The comparator’s hysteresis gives different switching operation for positive and negative values of the monitored current. Therefore, the gain of the instrumentation amplifier and the sensitivity of the hysteretic comparator directly control the threshold current \( I_{\text{thr}} \). Higher levels of hysteresis help lower inaccurate switching but put additional requirements on the gain needed from the differential amplifier and subsequent gain-bandwidth product limitations. The comparator must have fast response time and high slew rate in order to minimize delay during switching action. A LT1719 comparator from Linear Technology has fast 4.5ns response time, 2.2ns output rise time, 2.5ns output fall time, and rail-to-rail output to cleanly and accurately drive the MOSFET switches. Hysteresis in the comparator uses a positive feedback resistor between the output and non-inverting input and an input resistor from the non-inverting input to ground. Fig. 21 shows the hysteretic comparator topology used. Resistor choice follows equation 8 [15].

\[
R_1 = \frac{(R_2)(V_s - 0.6V)}{(\text{hysteresis})}
\]  

Eqn. 8 provides an approximation for resistor values. In
practice these values need some fine tuning to account for additional delay from the instrumentation amplifier, comparator, and switches. There is no single good choice for $R_1$ and $R_2$ because the desired hysteresis level depends on the gain of the instrumentation amplifier. Operating the circuit without feedback and viewing the switching waveforms led to values of $R_1 = 100k\Omega$ and $R_2 = 10k\Omega$. Fig. 41 shows simulation results performed in LTSPICE (see appendix). Fig. 22 shows the actual output for a sine wave input with no feedback and a 32Ω load. The switching events correspond to $I_{thr} = 15.6mA$ with the instrumentation amplifier’s gain set to 278 V/V. The relatively low output power of the circuit allows some freedom for the choice of $I_{thr}$ due to less spread between the highest and lowest switching frequencies. Higher output power decreases the power bandwidth of the switches but increases fidelity (see Section VII-A).

The comparator’s inverting output gives ±5V and controls the MOSFET switches. The LT1719 provides several additional functions not needed for this application such as the ability to provide different voltages for input and output. Extra pins are tied either high or low depending on their bypass requirements.

\[ A_v(new) = \frac{V_o}{V_{in}} \approx \frac{R_s + R_f}{R_s + \frac{R_s + R_f}{A_v} + \frac{R_s \times R_f}{A_v \times Z_{in}}} \] (9)

B. Switches

The Class D section ideally uses switches with low on resistance, fast response time, and good power handling, requirements easily met with power MOSFETs. The MOSFETs must have low $R_{on}$ to minimize power dissipation and high speed to handle the upper boundary of switching frequencies. The Vishay IRFU9024 P-channel power MOSFET has 0.28Ω on resistance with rise/fall times between 30-70 nS [13]. The ON Semiconductor NTD4904N N-channel power MOSFET has 3.7mΩ on resistance with rise/fall times between 10-30 nS [14].

C. Output Inductor

The switches connect to the speaker load through the inductor $L_1$. $L_1$ requires sufficient current carrying capabilities and low winding resistance. A threshold current of $I_{thr} = 20mA$ and maximum switching frequency of about 120kHz corresponds to an inductor value of $L_1 = 560\mu$H. An inductor with such a high value requires a large footprint and represents a major drawback to this circuit. Increasing the switching frequency decreases the size of the inductor but puts additional requirements on the switching network. For example, an inductor value of $L_1 = 20\mu$H increases the maximum switching frequency to about 35MHz, well above the bandwidth of the components used in this design.

Small electronics often avoid physical inductors by using operational amplifiers in Sallen-Key, general impedance-converter, or gyrator topologies. While these designs give good versatility and eliminate the need for bulky inductors, the current handling requirements make them unsuitable for this project. Moreover, the basic philosophy of a parallel amplifier hinges on avoiding inefficient push-pull output stages. The use of a simulated inductor would most likely consume enough power to make the efficiency gains of the parallel amplifier meaningless.

The inductor should have low resistance and sufficient current handling. A 560μH power inductor from Bourns has a DC resistance of 0.32Ω and maximum current rating of 1.9 amps.

D. AB Amplifier

Most low wattage AB amplifier ICs (and some opamps) work well for the AB section. While the overall design calls for a total output power of about 1W, the AB section primarily functions as a voltage source and only needs to provide a minority of the total power demand. The AB section controls the output voltage and requires good distortion figures. The ST Microelectronics TDA2822M stereo power amplifier has low 6mA quiescent current with < 0.2% total harmonic distortion + noise [11].

Input voltages higher than about 65mVpp begin to clip the TDA2822M. Fig. 23 shows how to lower the voltage gain of the AB amplifier using negative feedback. Eqn. 9 gives a calculation for the new voltage gain [17].
Fig. 23. Gain reduction technique for AB amplifier using negative feedback [17].

\[ A_v = 46 \text{dB} \]

\[ Z_{in} \]

\[ R_s = 1 \text{k}\Omega \]
\[ R_f = 10 \text{k}\Omega \]

A new input linear range of about 700mV.

E. Power Supply

The circuit requires a dual supply. Single supplies, such as those from batteries, offer much greater versatility. Fig. 24 shows an LT1210 current feedback amplifier used as a voltage follower. The output of the voltage follower creates a low-impedance virtual ground to turn a single supply into a dual supply. The two closely-matched resistors create a voltage divider at the non-inverting input to the buffer with \[ V^+ = \frac{V_0}{2} = V_0 \]. With a maximum 1.1A current output, this amplifier sinks or sources any required current from the circuit [16]. The LT1210 datasheet quotes an output impedance of 0.1\Omega at 100kHz. The nonzero ground impedance negatively affects operational amplifier performance, including decreasing the common-mode rejection ratio of the instrumentation amplifier.

A 12V, 1350mAh Ni-Mh battery used with an LM317 voltage regulator provides the regulated 10V supply voltage.

IX. Component Cost

Table I gives the cost of the individual components used in the circuit. The cost of all the components totals to $45.22. This does not include the cost of shipping, extra components ordered as backups or replacements, or extra components ordered during the component selection phase.

<table>
<thead>
<tr>
<th>Component</th>
<th>Cost</th>
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<tbody>
<tr>
<td>INA111AP Instrumentation Amplifier</td>
<td>$9.90</td>
</tr>
<tr>
<td>TDA2822M Dual Lo-Volt Power Amplifier</td>
<td>$1.62</td>
</tr>
<tr>
<td>LT1719 Comparator</td>
<td>$0.00 (free sample)</td>
</tr>
<tr>
<td>LT1210 Current Feedback Amplifier</td>
<td>$0.00 (free sample)</td>
</tr>
<tr>
<td>LM317 Voltage Regulator</td>
<td>$0.00 (salvaged)</td>
</tr>
<tr>
<td>IRFU9024 P-channel Power MOSFET</td>
<td>$1.19</td>
</tr>
<tr>
<td>NTD4904N N-channel Power MOSFET</td>
<td>$0.40</td>
</tr>
<tr>
<td>560\mu H 2100HT-561H-RC Bourns Power Inductor</td>
<td>$2.61</td>
</tr>
<tr>
<td>12V 1350mAh Ni-Mh battery</td>
<td>$15.00</td>
</tr>
<tr>
<td>BPS Prototyping breadboard</td>
<td>$8.00</td>
</tr>
<tr>
<td>BPS Prototyping solderable breadboard</td>
<td>$6.50</td>
</tr>
<tr>
<td>Speaker</td>
<td>$0.00 (salvaged)</td>
</tr>
<tr>
<td>Resistors, capacitors, etc</td>
<td>$0.00 (salvaged)</td>
</tr>
<tr>
<td>Total</td>
<td>$45.22</td>
</tr>
</tbody>
</table>

TABLE I

Cost of individual components.

X. Circuit Simulation

A circuit simulation performed in LTSpice verifies the basic operation of the amplifier. Appendix B shows all relevant data and graphs. Appendix C gives the Spice netlist used for simulations. Fig. 42 shows the output currents and voltages at 1kHz, well below the power bandwidth of the switches. The small current contributed by the AB amplifier takes the form of a sawtooth wave cycling between ±20mA. The form of the sawtooth results from the integrating nature of inductor L1. Fig. 43 shows the output currents and voltages at 3kHz input frequency, slightly above the power bandwidth of the switches. Notice that the switching frequency decreases to zero for parts of the cycle, forcing the AB section to output additional current. This increases the total power dissipation. Fig. 44 shows the output currents at 10kHz input frequency, well above the the power bandwidth of the switches. The AB section contributes much of the current.

XI. Construction

The circuit was first constructed on a BPS Prototyping breadboard. Stray capacitances should not appreciably affect circuit performance given the 10MHz operating frequency quoted by the manufacturer [18]. Please see Figs. 46-48 in Appendix D for pictures of the breadboard prototype.

The difficulty involved in the physical construction of the amplifier exceeded all worst-case expectations. The original design called for an LT1713 high speed comparator only available in a small SSOIC package. An attempt to use a high speed operational amplifier failed because of slew rate limitations. Other high speed comparators gave unreliable performance because of their lack of rail-to-rail output and the circuit came close to overheating multiple times due to shoot-through in the power switches. More simulation with an
LT1719 comparator with similar specifications to the original LT1713 gave encouraging results. Unfortunately, the LT1719 only comes in a small-outline surface mount package and didn’t fit into the dual-in-line spacing of the breadboard. A frustrating afternoon spent in the laboratory with a microscope returned the LT1719 with dead-bug leads that could interface more easily with the breadboard. This soon broke from mechanical stress. An SO-PDIP converter chip presented a better solution without sacrificing performance or physical integrity.

Switching transients in the output caused large amounts of distortion. Each switching event would temporarily introduce distortion into the power supply rails, negatively affecting the performance of both the AB and instrumentation amplifiers. This distortion would cascade through the current sensing network and cause additional unwanted switching events, compounding the problem. Several different capacitors placed near the supplies of each IC helped reduce high frequency transients and stabilize supply voltages. This dramatically (but not completely) reduced switching the presence of transients. Additional filtering at the input of the current sensing network helped reduce transients further. Please see Section VIII for additional information on the low-pass filter used at the input of the current sensing network.

Problems with clean switching and slow comparators translated into extremely inaccurate, unreliable switching events. This caused additional problems when trying to test the circuit because the switches often ended up sinking or sourcing high levels of current from the AB amplifier. This resulted in the AB section overheating and breaking, requiring additional replacement parts, time, effort, and money.

More problems with burned ICs occurred during circuit startup. The circuit takes about one second for the filtering ICs to charge and for all the individual amplifiers and comparators to come online. This left the switching section uncontrolled, leading to current spikes through the switch and into the AB amplifier. Adding a 10Ω resistor in series with inductor L₁ reduces the current through the switches during startup but severely lowers efficiency due to the voltage divider. This leads to a 24% decrease in efficiency for a 32Ω load (such as headphones) and a massive 62.5% decrease for the 6Ω speaker load used during testing. This represents the single biggest concession made during the project. The low efficiency numbers dictate at least a partial redesign of the circuit. Fig. 25 shows a charging circuit for the comparator. When tied to +Vs the comparator goes into shutdown mode, outputting zero volts with high output impedance. The RC section will put the comparator into shutdown at startup and slowly charge, eventually settling the shutdown pin to ground and activating the comparator. The time spent in shutdown depends on the RC time constant of the network. Time constraints prevented testing this solution.

The circuit started operating according to theory after successfully reducing switching transients and large current spikes. Well controlled, accurate switching events did not immediately lead to distortion-free output, however. Fig. 26 shows an example for a 300Hz sine wave input at 16mW output power. Ideally, the AB section sinks or sources all extraneous ripple current from the inductor, leaving the output voltage largely undistorted. In practice, the non-zero output impedance of the AB section causes some ripple current to flow through the load. The distortion at the output depends on the relative value of the threshold current Iₘₚ compared to the total current through the load. Eqn. 10 shows a rough approximation.

$$\text{Distortion} \approx \frac{I_{\text{thr}}}{I_{\text{load}}}$$

Fig. 45 shows simulation results with 42mW output power (see Appendix A). Low output power increases the approximation in Eqn. 10 and leads to higher distortion. Increasing the output power therefore results in a cleaner output signal.

The original breadboard prototype returned the results in Sections XII - XIV. The last goal of the project involved transferring the amplifier to a permanent circuit board using soldered connections and incorporating the battery and voltage regulator (power to the breadboard prototype came from a wired DC supply). The completed circuit board behaved extremely erratically, possibly resulting from the non-ideal...
behavior of the battery. High internal resistance in the battery would translate to diminished CMR in the instrumentation amplifier and higher transients along the DC supply rails. Time constraints prevented further debugging. Please see Figs. 49 - 52 in the Appendix for pictures of the final circuit board.

XII. TESTING AND CIRCUIT PERFORMANCE

Fig. 27 shows both the output voltage across the load (top) and the switching voltage (bottom) for a 300Hz sine wave input. The switching voltage taken from the gates of the switching section and appears inverted compared to the actual output. Distortion present on the output suggests reflections or transients introduced during the switching action (see Section XI). Fig. 28 shows a magnified version of the same signal along with introduced distortion. Note that the switching voltage changes frequency during the cycle. Fig.
and current sensing network present a constant drain on the battery, even with no output. Table II shows the individual power consumption for each additional component. The operational amplifier used to create the virtual ground consumes a particularly large amount of power. The power consumed by the AB amplifier, instrumentation amplifier, and comparator will not appreciably increase with load power. Increasing the output power to the load naturally increases efficiency while diminishing the relative power drain from the support circuitry.

### XIV. DISTORTION RESULTS

The inherent non-linear nature of amplifiers produces harmonic distortion at integer multiples of the applied fundamental frequency [2]. Several conflicting methods exist to calculate THD. Eqn. 12 gives THD as the ratio of the total power in the harmonics compared to the power in the fundamental frequency [19], [20].

$$THD = \frac{P_2 + P_3 + P_4 + \cdots + P_\infty}{P_1} = \sum_{n=2}^{\infty} \frac{P_n}{P_1} \quad (12)$$

Power can also be expressed as the sum of voltages squared. Eqn. 13 gives an equivalent calculation.

$$THD = \frac{V_2^2 + V_3^2 + V_4^2 + \cdots + V_\infty^2}{V_1^2} = \sum_{n=2}^{\infty} \frac{V_n^2}{V_1^2} \quad (13)$$

Confusingly, THD measurements sometimes quote a ratio using only voltages (Eqn. 14). Although not equivalent to Eqs. 12 and 13, Eqn. 14 expresses the same concept: how well an amplifier reproduces a signal without introducing harmonics.

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \cdots + V_\infty^2}{V_1^2}} = \sqrt{\sum_{n=2}^{\infty} \frac{V_n^2}{V_1^2}} \quad (14)$$

Manufacturers usually cite Eqn. 14 in literature [19]. Distortion measurements sometimes extend to total harmonic distortion + noise (THD+N). This includes power from additional noise such as intermodulation distortion (IM) and crossover distortion [19].

In practice, measuring the THD+N of a parallel amplifier requires a spectrum analyzer and sine wave generator with pure spectral content used as an input. The spectrum analyzer (a vintage Hewlett-Packard 3582) measures the output as a series of impulses corresponding to the frequencies causing distortion (see Fig. 34). With the fundamental frequency normalized to 0dB, the THD+N simplifies to the sum of the relative dB in the harmonics (Eqn. 13), or the square root of the sum (Eqn. 14). These measurements lend themselves easily to calculations programs such as Microsoft Excel (see

### TABLE II

<table>
<thead>
<tr>
<th>Component</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
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</thead>
<tbody>
<tr>
<td>AB Amplifier</td>
<td>6</td>
<td>60</td>
</tr>
<tr>
<td>Instrumentation Amplifier</td>
<td>4</td>
<td>40</td>
</tr>
<tr>
<td>Comparator</td>
<td>4</td>
<td>40</td>
</tr>
<tr>
<td>Virtual ground and voltage regulator</td>
<td>40</td>
<td>300</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>54</strong></td>
<td><strong>540</strong></td>
</tr>
</tbody>
</table>

**QUIESCENT POWER OF CIRCUIT WITH NO OUTPUT.**
Fig. 34. Sample data taken from spectrum analyzer during THD measurement.

Fig. 35. Example Excel calculations for THD+N measurements.

Fig. 36. Total harmonic distortion + noise (%) for the parallel amplifier at \( P_{\text{out}} = 0.5\,\text{W} \) and \( P_{\text{out}} = 0.9\,\text{W} \), along with results from the class A amplifier at \( P_{\text{out}} = 0.5\,\text{W} \) for comparison. The bandwidth is 25kHz.

<table>
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<tr>
<th>Harmonic</th>
<th>Power</th>
<th>dB</th>
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<tr>
<td>2</td>
<td>-43.9</td>
<td>4.0738E-05</td>
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<tr>
<td>3</td>
<td>-54.9</td>
<td>3.2359E-06</td>
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<td>4</td>
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<td>7</td>
<td>-72.2</td>
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<td>8</td>
<td>-100</td>
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<tr>
<td>9</td>
<td>-73</td>
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<tr>
<td>10</td>
<td>-100</td>
<td>1E-10</td>
</tr>
<tr>
<td>11</td>
<td>-100</td>
<td>1E-10</td>
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<td>12</td>
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<td>15</td>
<td>-100</td>
<td>1E-10</td>
</tr>
<tr>
<td>18700</td>
<td>-53</td>
<td>5.0118E-06</td>
</tr>
</tbody>
</table>

Total (by power) \( 5.05507E-05 \)  
THD % by voltage \( 0.710990228 \)

The results in Fig. 36 show THD+N calculated with Eqn. 14 taken from the parallel amplifier at a range of frequencies at two different output powers, along with the THD+N of the class AB amplifier alone for comparison. Interestingly, THD+N taken from the AB amplifier at \( P_{\text{out}} = 0.9\,\text{W} \) returned essentially unmeasurable results, consistent with the manufacturer’s claim of THD+N \( \leq 0.2\% \) (probably below the capabilities of the spectrum analyzer).

XV. Conclusion

The low efficiency results prevent this circuit from replacing traditional amplifiers. These numbers stem from the execution of the circuit and not the theory behind the design itself. A more successful design should include better control over switching, more accurate sensing of threshold current, and some sort of monitoring system to prevent the switches from overloading the AB section in case of malfunction. The latter function might possibly use the output voltage of the current sensing amplifier and the shutdown pin of the hysteretic comparator. An improved current sensing scheme could move the sensing resistor \( R_{\text{sense}} \) to one of the power rails of the AB amplifier, removing it directly from the output section. A more sophisticated hysteretic comparator topology would produce more accurate switching events and improve distortion.

The large footprint of the output inductor probably prohibits this amplifier from use in small electronics as originally proposed. Low- and mid-frequency operation at low output powers requires a large-value inductor in the range of 100-1000\( \mu \)H. These large inductors correspond to bulky coils up to 1” diameter. This obviously presents a challenge when attempting to incorporate the design into portable devices. Although techniques exist that replace physical inductors with amplifier structures (such as Sallen-Key or generalized impedance converters), this defeats the purpose of replacing the AB section with high-efficiency switches by making the switching section dependent on yet another push-pull output section with nonzero quiescent current.

Despite drawbacks, the self-oscillating parallel amplifier rests on a solid - if somewhat nonintuitive - idea. Self-oscillation presents a slightly different challenge conceptually compared to more traditional class D designs because of the nontraditional use of feedback. The finished amplifier required knowledge of audio systems, power supply design, frequency response, filters, and small signal analysis. Skills related to the physical construction of circuits, project planning, the organization of datasheet information, and the accuracy and reliability of testing methods all improved as time progressed. Finally, the amplifier represented an almost poetic undertaking by requiring the author to work through frustrations and setbacks and continually requiring further knowledge and insight into analog design.

Improved designs of a self-oscillating parallel amplifier should increase the output power to reduce distortion and increase efficiency. Higher output power reduces the relative magnitude of the threshold current while also giving more choice to designers regarding switching frequency and bandwidth. While the large inductor really prevents this amplifier...
from entering the world of portable electronics, a physically large amplifier would reduce the need for small components. The only major modifications needed to increase output power are higher source voltages and the increased current handling for the switches and inductor.

REFERENCES


ACKNOWLEDGMENTS

The author would like to thank Dr. David Braun for his guidance and help throughout the project, and Mark Stambaugh for his many years of unsolicited, unfiltered wisdom.

Max Ullrich is a graduating senior from Cal Poly, San Luis Obispo. He listens to an inordinate amount of music.
## APPENDIX A

### PROJECT TIMELINES

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<td>Week 1</td>
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<td>Week 4</td>
<td>Week 5</td>
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<td>Circuit Design</td>
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<td>Excel simulations</td>
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<tr>
<td>Documentation</td>
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<tr>
<td>Construction</td>
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<tr>
<td>Initial IC testing (Class AB and B amplifier)</td>
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<td>Comparator testing</td>
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<td>Power supply filtering</td>
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<td>Switches and feedback</td>
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<td>Troubleshooting, fine tuning</td>
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<td>Efficiency</td>
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<td>Total Harmonic Distortion</td>
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<tr>
<td>Final Documentation</td>
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</tbody>
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Fig. 37. Actual project timeline for self-oscillating parallel amplifier.
Fig. 38. First proposed timeline for completion of parallel amplifier design project.

Fig. 39. Second, slightly shorter proposed timeline for completion of parallel amplifier design project.
APPENDIX B
SPICE SIMULATION FIGURES

Fig. 40. Final circuit schematic.

Fig. 41. Simulation results for hysteretic comparator. Switching events occur at ±430mV.
Fig. 42. Output voltages and currents at $f_{in} = 1$khz

Fig. 43. Output voltages and currents at $f_{in} = 3$khz
Fig. 44. Output voltages and currents at $f_{\text{in}} = 10\text{kHz}$

Fig. 45. Output voltages and currents at $f_{\text{in}} = 1\text{kHz}$ and $P_o = 42\text{mW}$. Notice large threshold current compared to load current.
APPENDIX C
SPICE NETLIST

* G:\Class\Senior Project\Spice Model\Newest_Spice\parallel_amplifier.asc
Q1 Vcc N005 N006 0 CA3086
Q2 Vee N007 N006 0 CA3127
Q3 N005 N005 Vi 0 CA3086
Q4 N007 N007 Vi 0 CA3127
R1 Vcc N005 500
R2 N007 Vee 500
V1 Vcc 0 5
V3 Vi 0 SINE(0 3 1000)
Rload Vo 0 6
Rsense N006 Vo 0.1
V2 0 Vee 5
M1 Vswitch N001 Vcc Vcc CMOSP
M2 Vswitch N001 Vee Vee CMOSN
L1 Vswitch Vo 0.56m Rser=1
XU3 N002 N004 Vcc Vcurr LT1213
R5 Vo N004 1k
R8 N006 N002 1k
R9 Vcurr N004 500k
R10 0 N002 500k
XU1 Vcc N003 Vcurr Vee Vee Vee N001 Vcc LT1719
R3 N003 0 10k
R4 N001 N003 100k
.model NPN NPN
.model PNP PNP
.lib C:\PROGRA~1\LTC\LTSPIC~1\lib\cmp\standard.bjt
.model NMOS NMOS
.model PMOS PMOS
.lib C:\PROGRA~1\LTC\LTSPIC~1\lib\cmp\standard.mos
.model CA3127 PNP
+ (IS = 3.20E-10 XTI= 3.000E+00 EG = 1.110E+00 VAF = 1.00E+04
+ VAR = 1.000E+04 BF =1000E+07 ISE = 20.586E-12 NE = 1.990E+00
+ IKF = 61.500E-03 XTB = 0.000E+00 BR = .1000E+00 ISC = 10.805E-9
+ NC = 2.000E+00 IKR = 10.00E-03 RC = 10.000E+00 CJC = 281.1E-15
+ MJC = 0.138E-00 VJC = 0.7500E-00 FC = 5.000E-01 CJE = 651.9E-15
+ MJE = .336E-00 VJE = 0.750E-00 TR = 10.000E-09 TF = 122.61E-12
+ ITF = 1.600E-00 XTF = 2.050E+03 VTF = 307.00E+00 PTF = 0.000E+00
+ RE = 0.0E+00 RB = 0.00E+00
.tran 0 2m 0 1u
.model CA3086 NPN
+ (IS = 10.0E-13 XTI= 3.000E+00 EG = 1.110E+00 VAF = 1.00E+04
+ VAR = 1.000E+04 BF =1000E+07 ISE = 20.586E-12 NE = 1.990E+00
+ IKF = 61.500E-03 XTB = 0.000E+00 BR = .1000E+00 ISC = 10.805E-9
+ NC = 2.000E+00 IKR = 10.00E-03 RC = 10.000E+00 CJC = 281.1E-15
+ MJC = 0.138E-00 VJC = 0.7500E-00 FC = 5.000E-01 CJE = 651.9E-15
+ MJE = .336E-00 VJE = 0.750E-00 TR = 10.000E-09 TF = 278.55E-12
+ ITF = 1.770E-00 XTF = 91.38E+00 VTF = 18.37E+00 PTF = 0.000E+00
+ RE = 0.0E+00 RB = 0.00E+00
.model CMOSN NMOS LEVEL=3 PHI=0.600000 TOX=2.120000 UO=591.7 THETA=8.122000 RSH=8.545000 GAMMA=0.5863
+NSUB=1.98E+12 VMAX=1.733000+05 ETA=4.368000-02
+KAPPA=1.396000-01 CGDO=4.0241E-10 CGSO=4.0241E-10
+CGBO=3.6144E-10 CJ=3.8541E-04 MJ=1.1854 CJSW=1.3940E-10
+MJSW=0.125195 PB=0.800000
.MODEL CMOSP PMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
+TPG=-1 VTO=-0.9056 DELTA=1.5200E+00 LD=2.2000E-08 KP=2.9352E-00
+UC=180.2 THETA=1.2480E-01 RSH=1.0470E+02 GAMMA=0.4863
+NSUB=1.8900E+16 NFS=3.46E+12 VMAX=3.7320E+05 ETA=1.6410E-01
+KAPPA=9.6940E+00 CGDO=5.3752E-11 CGSO=5.3752E-11
+CBO=3.3650E-10 CJ=4.8447E-04 MJ=0.5027 CJSW=1.6457E-10
+MJSW=0.217168 PB=0.850000
.lib LTC.lib
.backanno
.end
APPENDIX D
PROJECT PICTURES

Fig. 46. Breadboard prototype.

Fig. 47. Breadboard prototype.
Fig. 48. Breadboard prototype.

Fig. 49. Final circuit board.
Fig. 50. Final circuit board showing AB amplifier (left), instrumentation amplifier (middle), and hysteretic comparator (right).

Fig. 51. Final circuit board showing inductor and output switches (right).
Fig. 52. Final circuit board showing virtual ground (left) and voltage regulator (right).

Fig. 53. The author hard at work taking THD measurements.