

A High Power, High Efficiency Amplifier using GaN HEMT

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Abstract—A class B and a class F power amplifier are described using a GaN HEMT device. They both were designed to operate at a frequency of 1.7 GHz with the same bias conditions. The performances of each amplifier were successfully simulated and compared. A class B amplifier was physically implemented and achieved a high power-added-efficiency of 69.2%, 39.9 dBm output power and associated gain of 14.9 dB. The experimental results were in close agreement to the simulation results.

Index Terms—Power Amplifier, High Power, High Efficiency, GaN HEMT, Power Added Efficiency.

I. INTRODUCTION

Wireless communication systems demand low-cost, high-efficiency, and compact amplification solutions. The final RF power amplifier stage is known to be one of the most critical and power-consuming building blocks. There has been a significant effort to increase the efficiency of power amplifiers [1]. This work utilizes highly efficient GaN power transistors and compares their power-added efficiency performance in both class B and class F circuit configurations.

A. Power Added Efficiency for Class B and F amplifiers

Power added efficiency (PAE) is the ratio of the difference between RF output power and input power divided by the DC power [2]. Power amplifiers are categorized by different classes of amplification (A, B, AB, C, D, E, F, F⁻¹, and S). The classes of operation differ in method of operation, efficiency, linearity, and power-output capability. The classes are categorized according to the conduction angle of the transistor. As the conduction angle of the drain/collector of the transistor decreases, the efficiency of the amplifier increases. For example, the maximum ideal efficiency of class A amplifier is 50% while the ideal efficiency of class B is 78.5%.

Of all different classes of amplifiers, class F is recognized as the most efficient. Class F amplifiers can achieve 100% efficiency by using harmonic resonators in the output network to shape the drain/collector waveforms such that the load appears to be a short at even harmonics and an open at odd harmonics. The drain/collector voltage waveform includes one or more odd harmonics to approximate a square wave, whereas the drain/collector current waveform includes one or more even harmonics to approximate a half a sine wave [3]. Because there is no time overlap between

the drain/collector voltage and current waveform, a maximum drain efficiency of 100% can be achieved.

B. GaN HEMT

The efficiency of the amplifier is limited by the characteristics of the transistor. The maximum efficiency of 100% of a class F amplifier can only be achieved by assuming that the transistor is an ideal current source. Among the many different device types, GaN HEMT devices seem to be promising for high power amplifiers. GaN HEMTs have a very large material band gap which permits them to be operated at high drain voltages and high power density [4]. Thus, smaller devices can be used to achieve a given power level. For this experiment, a GaN HEMT was chosen as the device and both class B and class F operations were compared. Section II provides simulation results of the comparison of GaN power amplifier performance in both class B and Class F configurations. Section III highlights the experimental results for a fabricated class B amplifier.

II. SIMULATION

A. S-Parameters and modeling

The class B and F simulations were performed using Agilent’s Advanced Design System (ADS). For this particular design, a packaged GaN HEMT from Cree, Inc. (CGH40010) was chosen and the device model was provided by the manufacturer. To verify that the model provided an accurate representation of our device samples, small signal scattering parameters generated from ADS were compared to the ones given in the datasheet (Table I). Close agreement was shown.

Table I. S-parameters of a GaN transistor with bias condition of $V_{DS}=28V$ and $I_{DQ}=100mA$, at 1.7GHz

	S11	S12	S21	S22
Simulation	0.872/	0.034/	4.017/	0.634/
	174.712 ⁰	-7.596 ⁰	68.974 ⁰	172.522 ⁰
Datasheet	0.862/	0.0395/	3.96/	0.5926/
	175.86 ⁰	-10.35 ⁰	68.15 ⁰	177.14 ⁰

B. Load and Source Pull Analysis

After confirming small-signal agreement with the datasheet, load and source pull analyses were performed to obtain the output power and PAE contours of the transistor using a harmonic balance analysis. The load-pull and source-pull analyses provided both the input and output impedance of the transistor for the conditions of maximum PAE in both class B and Class F configurations. For the class B load-impedance case, an impedance value of $14.46+j22.72 \Omega$ will provide 72.95% PAE and 38.87 dBm power delivered. A source impedance value of $2.08+j4.58 \Omega$ will provide the best PAE and output power. Then, both input and output matching networks were designed to directly match these impedances. For both class B and class F analyses, an input signal frequency of 1.7 GHz with power of + 25 dBm is applied while the transistor is biased at $-2.7V V_{gs}$ and $28V V_{ds}$. These input conditions were consistently used in the design of the overall amplifier comparison.

C. Class B and Class F results

The input and output impedance matching design used 50 ohm impedance microstrip transmission lines. The board material was RT Duroid® with relative dielectric constant of 2.33 and substrate thickness of 0.78 mm (31 mils). The simulation results focus on the drain voltage and current waveforms, the load voltage and current waveforms, fundamental power delivered to the load, drain efficiency, and PAE. The class B amplifier design involves biasing the transistor at or near cut-off and designing the input and the output matching networks according to the impedances achieved from the load and the source-pull analyses. The results of the class B power amplifier simulation are shown in Fig.1. This figure shows the voltages and currents at the device drain and at the amplifier load for the class B design. With an input power of 25 dBm and DC supply power of 13.60 W, the output power is 10.87 W (40.36 dBm). This gives a PAE of 77.56%.

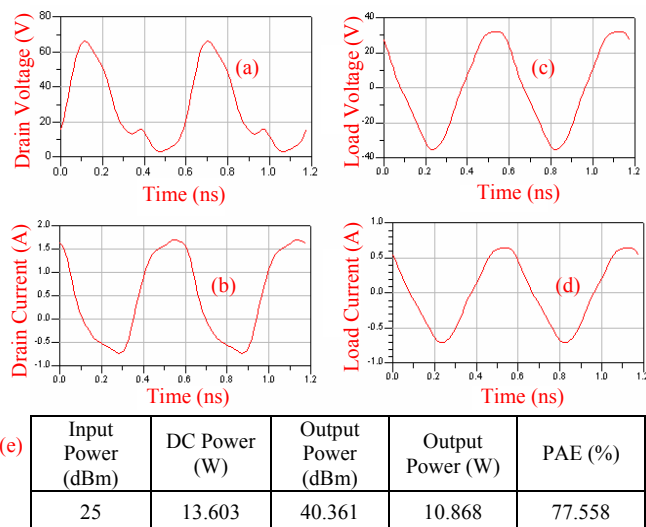


Figure 1. Simulation Result of Class B Power Amplifier: (a) Drain Voltage Waveform, (b) Drain Current Waveform, (c) Load Voltage Waveform, (d) Load Current Waveform, and (e) Final Results

The class B amplifier is biased near cutoff. When the amplifier is operating in the cutoff region, harmonics are introduced in the drain. This distorts the drain voltage and current waveforms to reduce the overlap in time between the voltage and current peaks. This voltage to current phase inversion reduces the amount of power being dissipated in the drain of the amplifier and produces high-efficiency amplification.

Another amplifier was designed to operate in class F to compare the results with that of class B operation. The class F amplifier differs from the class B design with addition of two resonant tanks circuits at both the input and at the output of the transistor. The values of the tank circuits are calculated from the equations given in reference 5. The class F amplifier simulation results are given in Fig. 2.

Class F amplifiers are usually biased near cutoff similar to class B amplifiers. Thus, to compare the results of different classes of operation of the amplifier, the matching networks that were already designed for class B operation in Fig. 1 remained unchanged. The class F resonator circuit is added to the input side before the input matching network. Another resonator was added to the output side after the output matching network for class F operation. Finally, only the resonator circuit element values are optimized to achieve the highest PAE.

The results of the class F amplifier simulation show that the power delivered is 40.73 dBm, DC power is 13.81 W, and the PAE is 83.33%. As the theory indicates, class F operation has slightly greater PAE than that of class B operation. The increase in efficiency can be traced to an increase in fundamental frequency power delivered to the output. The DC power has also increased slightly, but the delivered RF power had a greater contribution to the overall increase in PAE. The increase in the output delivered power is from the improved linearity of the output curve (c and d from Fig. 2).

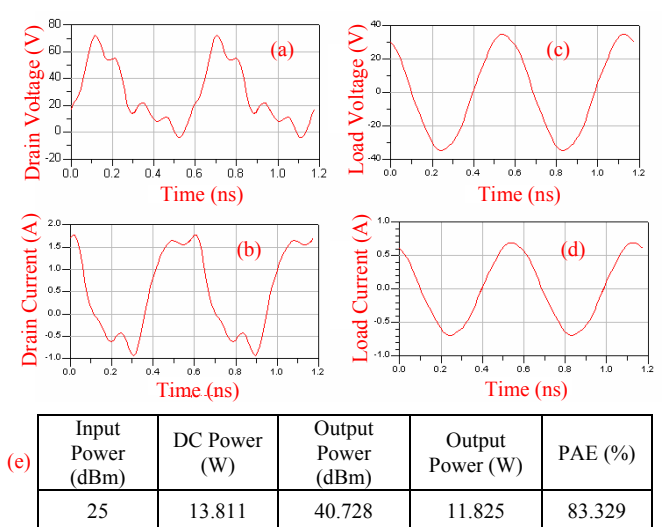


Figure 2. Simulation Result of Class F Power Amplifier: (a) Drain Voltage Waveform, (b) Drain Current Waveform, (c) Load Voltage Waveform, (d) Load Current Waveform, and (e) Final Results

The class F load voltage curve displays an improved sinusoidal waveform shape compared to class B operation. Less power is being provided to the harmonic frequencies. Class F operation traps the harmonic energy into the drain of the transistor. However, a disadvantage of class F operation is the additional complexity of adding the resonator elements into the design and fabrication process.

III. EXPERIMENTAL RESULTS

A. Construction

The design is fabricated on an RT Duroid® board with height of 0.78 mm (31 mils) as is specified in the simulation. The amplifier design is illustrated in Fig. 3. The GaN HEMT device was mounted to an Aluminum heat sink below the board. The overall dimensions are 76.2 mm x 127 mm (3" x 5"). Four chip 100 pF DC blocking and bypassing capacitors and two 1 uH wire-wound RF-chokes were used to DC bias the transistor. The output of the amplifier was terminated in a high power 50 ohm attenuator to provide a good 50 ohm load match. The output was observed both with a calibrated power meter and a spectrum analyzer.

B. Final Results

The final results of the class B power amplifier provided an output power of 39.91dBm with a DC supply power of 13.71W. This calculates to a PAE of 69.22%. This result is obtained with a bias condition of -2.7V V_{gs} and 28V V_{ds} . The summary of the results obtained from the simulation and the actual experiment is described Table II.

The amplifier PAE varies with the drain voltage and gate bias. An effort was made to find the sensitivity to bias conditions for this amplifier. Both drain efficiency and PAE are plotted versus the drain voltage in Fig. 4.

Fig. 4 shows that as the drain voltage is varied, the drain efficiency stays relatively constant, but PAE has a stronger dependency. This deviation is due to the output power. As drain voltage is increased, a greater output power is observed. But once the transistor power completely saturates, output power no longer increases and PAE is decreased. The plot shows that the highest PAE is achieved when drain voltage is biased at around 30 V.

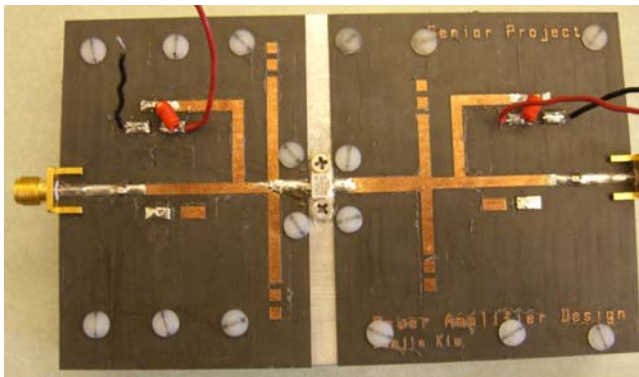


Figure 3. Class B Power Amplifier.

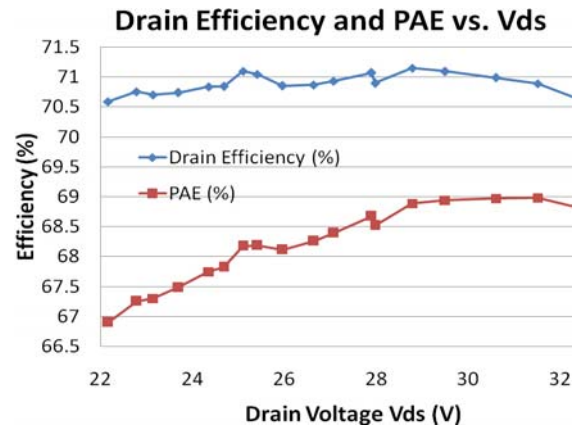


Figure 4. Drain Efficiency and PAE as a function of Vds for a class B Power Amplifier. The gate bias is held constant at -2.7V.

The amplifier efficiency also depends on the input power. Fig. 5 shows the power sweep curve as well as the corresponding PAE. As the input power is swept from 23 dBm to 25.5 dBm, the output power increases fairly linearly, indicating that over this range of input powers, the amplifier has a constant gain.

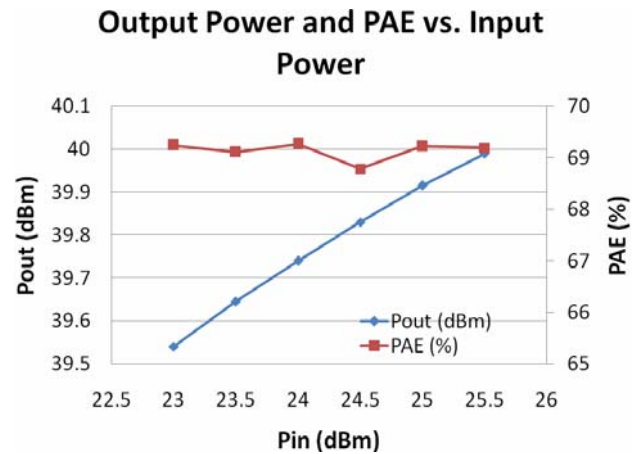


Figure 5. Output Power and PAE as a function of Input Power of Class B Power Amplifier: Pin is varied from 23 dBm to 25.5 dBm

Table II. Comparison between Simulated Results and Experimental Results

	DC Power (W)	Output Power (dBm)	Output Power (W)	PAE (%)
Class B Simulated	13.60	40.36	10.87	77.56
Class F Simulated	13.81	40.73	11.83	83.33
Class B Experimental	13.71	39.91	9.81	69.22

IV. CONCLUSION

The simulation results show that the class B power amplifier can achieve up to PAE of 77%. This result is compared to the actual fabricated board, which achieves a PAE of 69.22%. The simulated results comparison between the class B and the class F showed a moderate increase in PAE for the class F operation compared to class B. In conclusion, whether the operation of the amplifier is class B or class F, GaN HEMT transistors with good modeling and circuit fabrication can prove to be very efficient. Future work will provide a more thorough experimental comparison between class B and class F amplification.

ACKNOWLEDGMENT

Thanks to Cree, Inc. for providing GaN transistors and the device models. Professor Dean Arakaki at Cal Poly provided the microstrip circuit fabrication facility.

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