INTELLIGENT IRRIGATION ZONE SPLITTER

by

David Boeck

Senior Project

ELECTRICAL ENGINEERING DEPARTMENT

California Polytechnic State University

San Luis Obispo

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Abstract

The intelligent irrigation zone splitter allows easy expansion of an existing irrigation controller. To expand on an existing controller a new wire is needed to run between the controller and the valve. This path may be buried beneath driveways, patios, and sidewalks. The intelligent irrigation zone splitter uses an already existing wire path to control two valves and create a new watering zone. This controller uses timing and memory to split the total watering time of the zone.

I.   Introduction

Existing irrigation systems are limited to expansion. Adding an additional irrigation zone may be needed if lawn area increases or if a drip water irrigation system is installed for potted plants. Adding additional sprinkler heads or drip valves may not be possible because of limited water pressure, thus a new zone must be created. However, adding a new irrigation zone requires an extra wire connected from a valve to the controller. This cable path may be buried beneath driveways, patios, and sidewalks. Because of this complication, laying new cables to the existing controller may be an expensive and unwanted cost.

In order to avoid connecting a wire from the valve to the controller an intelligent irrigation zone splitter controller at the valves is needed. This controller would take one remotely controlled zone and divide it up to two locally controlled zones. The controller would split the overall watering time in half between the two zones. The circuit would use the previous watering period to calculate the next watering cycle time. Zone 1 would be split into zone 1a (previously zone 1) and 1b (previously zone 2), and zone 2 would become free for an additional valve. The main controller would be set for twice the desired time and the zone splitter controller would divide the watering time equally between the two zones.

II.   Background

A sprinkler irrigation controller is a water management tool designed to operate a home watering system. Multiple wires run from the controller to each of the sprinkler valves that need to be controlled. Each valve needs its own wire feed from the controller for individual operation. A time and duration is set for each valve. At the appropriate time a $24V_{rms}$ signal is sent to the valve to open it. The water pressure sends the water through the sprinkler heads of that zone. The valve is open for the duration of the signal and closes when the signal is released.
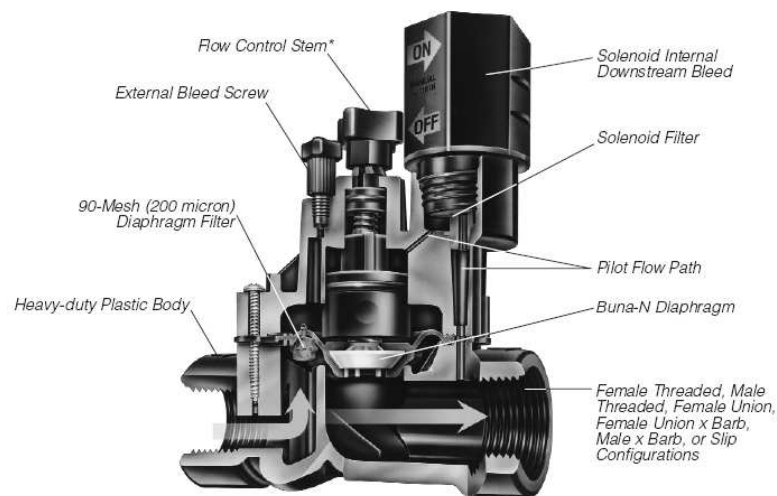

Figure 1: Sprinkler Valve Cross-Section

The cross-section of a sprinkler valve is shown in Figure 1. When power is not applied to the solenoid the diaphragm is closed and water does not flow through the valve. There is a small hole in the diaphragm that leaks water into a middle chamber

The water in the middle chamber has a water pressure greater than the water line; thus, the valve stays closed. When AC voltage is applied to the solenoid, a magnetic field pulls a pin from the middle chamber releasing the pressure. The water line pressure become greater than the water pressure in the middle chamber and the diaphragm opens. When power is disconnected the pin closed and water pressure in the middle chamber closes the valve.

III. Requirements

The 24V$_{rms}$ source powers the device, sets the clock base, and drives the solenoids of the valves. The controller divides the watering time evenly between the two valves. The controller will use the previous watering cycle to determine the next watering cycle. The controller enables the first valve for half the previous total watering time, while the second valve is enabled for the remaining time. Therefore, if the total watering time is constant during repeated use then the watering time between the two valves will be divided evenly. A 30 second delay in the write sequence is necessary to prevent writing during zone cycling in the main controller. The controller needs to run for at least 2 hours for a maximum watering time of 1 hour per valve. The controller will operate outside and will be exposed to a range of temperatures. The controller needs to operate between 0°C and 60°C. The controller needs to be protected by power surges and short circuits.

The clock is based on the 24V$_{rms}$ 60Hz line. An up counter measures the total watering time of the two zones. This value is stored in a non-volatile EEPROM latch when the 24V$_{rms}$ power is removed. At startup a down counter latches the data stored in the EEPROM and valve one is enabled. When the down counter reaches count zero it disables valve one and enables valves two. The clock frequency of the down counter needs to be twice the frequency of the up counter, thus splitting the stored time in half. Valve one would be enabled for one half the previous watering time.

To program the controller an initial calibration run is necessary. For the initial run, the first valve would be on for half the previous watering time or the current watering time depending on which is less. The second valve will run for the remaining period if time exists. After this initial calibration, the controller would be calibrated for the required watering time. If the total watering time is changed, then a new calibration run is needed before normal operation.

IV. Design

To design a system a block diagram or flow chart should be created. Figure 2 shows the flow chart of the irrigation controller. The input to the controller is the $24V_{rms}$ AC line. The protection consists of surge and current limiting protection at the input connections. The rectifier and bias supply converts the input AC voltage to power all DC circuitry. The detector detects the 60Hz component of the AC input to derive a clock. The clock base changes the 60Hz to an appropriate clock frequency. The up counter counts to time the event and the value is reseted on startup. The EEPROM stores the time period of the up counter when the power is removed. The power fail detects when the input voltage is removed to strobe the EEPROM. The down counter controls the valve control and its time period is stored from the EEPROM at startup. The valve control circuit powers the valves, and it includes current limiting protection from shorted valve and surge protection on the output connections.

Digital logic controls the EEPROM and counters used in the flow chart. Complementary MOSFET (CMOS) logic was used because it has virtually zero static power dissipation. More specifically, CMOS logic draws little current in its steady state. Therefore, the linear voltage regulator used to power the logic circuits will dissipate little power because the load current is low.
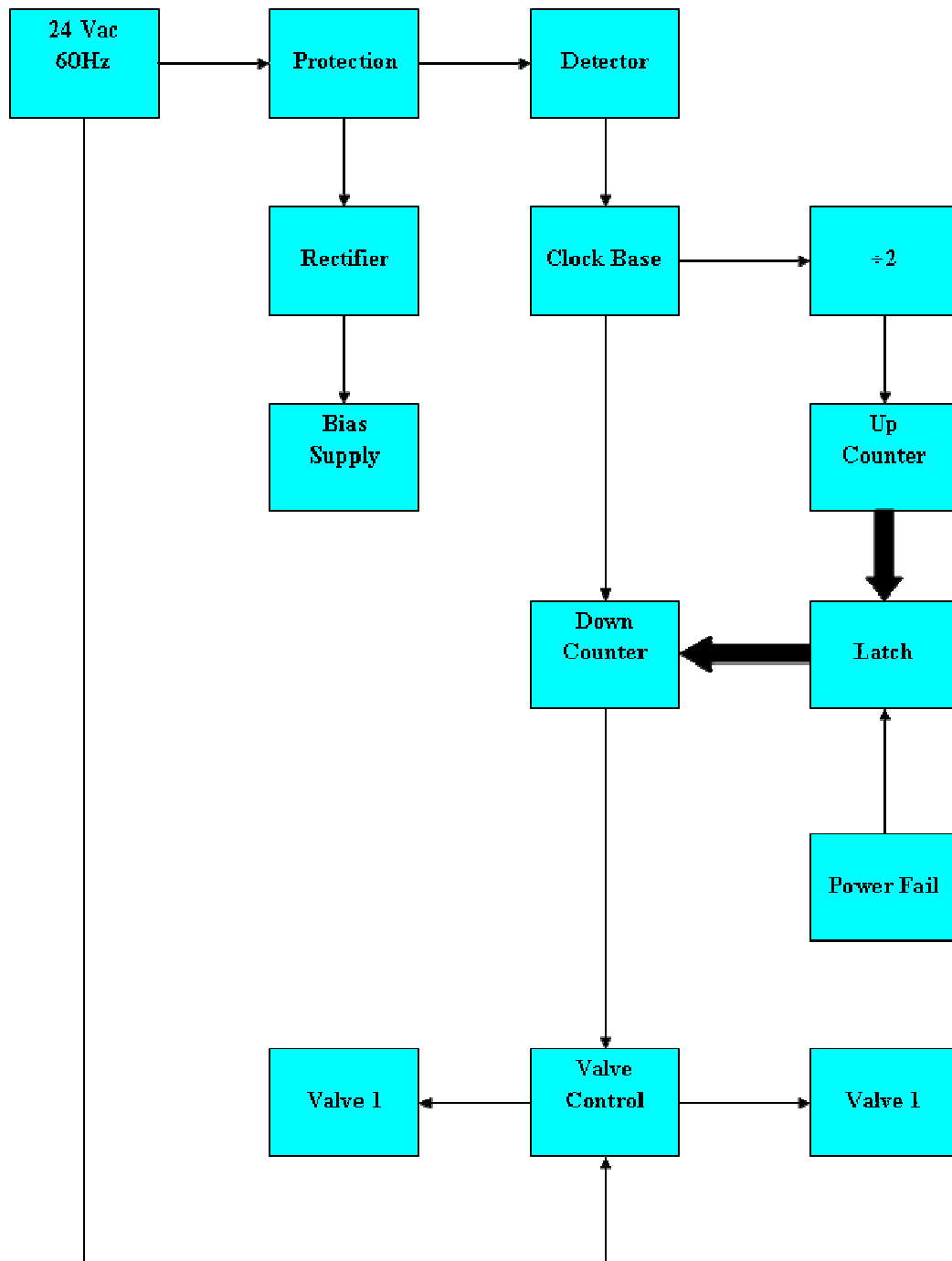
Figure 2: Flow Chart of Irrigation Controller

The integrated circuits were chosen from the 74HC families which are high-speed CMOS logic circuits. All IC packages were dual-in-line packages (DIP) for the ease of breadboard testing. The 74HC40103, 8-stage synchronous down counter, was chosen for the down counter. The counter can latch the data asynchronously for the controller design. The 74HC590, 8-bit binary counter with 3-state output register, was chosen for the up counter. The high impedance (Hi-Z) state ensures that the up counter does not affect the asynchronous latch from the EEPROM at start up. The CAT28C64B, 64K-bit CMOS parallel EEPROM, was chosen for the EEPROM latch. Even though only one address register is necessary for the controller, this was the cheapest EEPROM with a low power standby mode, DIP package, 8-bit register, and parallel loading. The EERPOM operates at a 5V supply, therefore the rails of the controller was set to 5V. When the chip is enabled the biasing current is 25mA, whereas when the chip is in standby the biasing current is 100μA. For this reason, the EEPROM operates in standby mode during normal operation to conserve power.

The 8-bit data line between the up counter, the down counter, and the EEPROM form a bus. During start up the controller disables the output of the up counter while enabling the output of the EEPROM. The down counter then latches the data from the EEPROM. At power fail the controller enables the output of the up counter and the EEPROM latches the data from the up counter. However, during normal operation, not in start up or power fail, both outputs would be in Hi-Z and the bus would be in an unknown state during this time. Pull up resistors would pull the value high during Hi-Z and prevent the unknown state form occurring. A 47kΩ

series-in-line (SIL) resistor array would achieve this pull up and limit the current
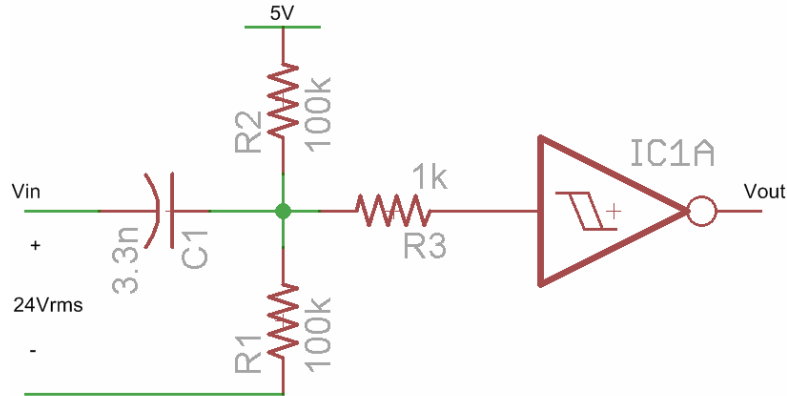
drawn when the data is low.

Figure 3: Frequency Detector

The frequency detector converts the 60Hz $24V_{rms}$ sine wave to a 60Hz $5V_{pp}$

square wave. Figure 3 demonstrates the circuit that accomplishes this. Capacitor C_1

provides AC coupling of the $24V_{rms}$ sine wave and provides attenuation. Resistors R_1

and R_2 provided DC offset to shift the attenuated signal between 0V and 5V. These

two resistors must have equal resistances to apply the 2.5V offset. Resistor R_3 applies

current limiting to the internal protection diodes of the CMOS gate. This added

protection ensures that the input current does not overstress the protection diodes

when the voltage becomes greater or less than the supply rails. This becomes a

possibility when driving a CMOS gate from a different supply. A Schmitt trigger uses

hysteresis to eliminate comparator chatter. A slow varying signal tends to produce

multiple output transition because of AC noise within the signal. The 74HC14, hex

inverting Schmitt trigger, was chosen for the logic gate.

Assuming the Schmitt trigger has infinite input impedance, the AC equivalent of Figure 3 is C_1 in series with R_1 and R_2 in parallel. The resistor values R_1 and R_2 were chosen to reduce the DC current and allow an attainable capacitance for C_1. The function of C_1 attenuates the $24V_{rms}$, $33.9V_p$, input voltage to a $2.5V_p$ sine wave. A capacitor value of 3.91nF would achieve this attenuation at 60Hz; therefore, a standard value of 3.3nF was chosen. Because this is a frequency detector, the phase shift caused by the capacitor is inconsequential.

The controller must divide the 60Hz clock frequency in order for the counter to measure a watering cycle of at least 2 hours. This requires the maximum 256 states of the 8 bit register to be greater than 2 hours or 7200 seconds. The period must be greater than 28.1 seconds. Dividing the 60Hz clock by 2^{11} would achieve a period of 34.1 seconds. The 74HC4040, 12-stage ripple-carry binary counter, was chosen to divide the clock by 2^{11} for the up counter and 2^{10} for the down counter.
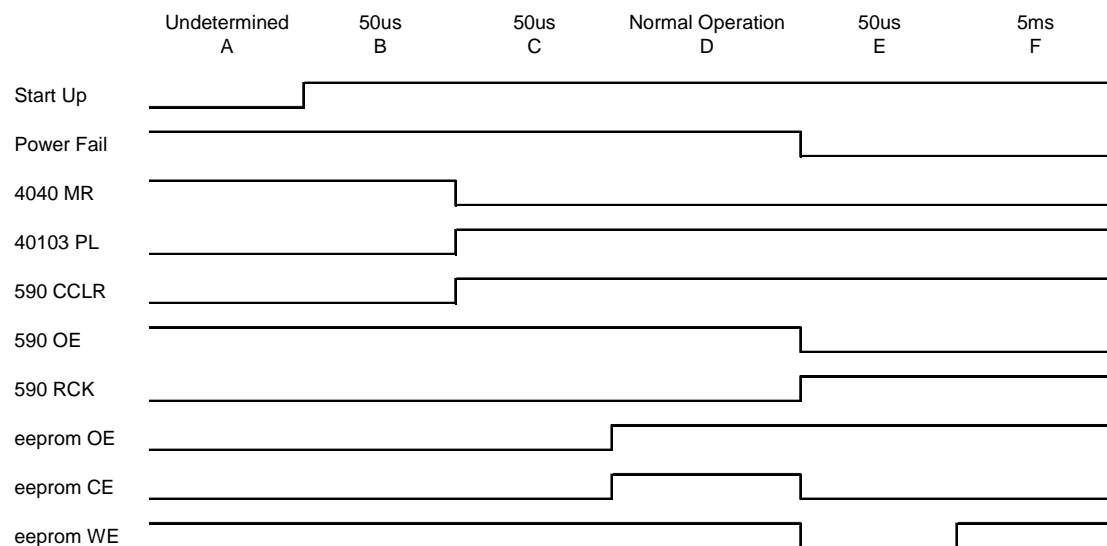

Figure 4: Timing Diagram

The timing diagram for the controller is displayed in Figure 4. The ripple counter, up counter, down counter, and EEPROM must be triggered correctly for the controller to operate. The start up signal goes high when the supply rails reach 5V. The power fail signal goes low when power is removed from the device. State A is the time before the supply rails become established when the device initially turns on; thus, this state is undetermined. During state B the start up is initiated, the ripple counter is reseted, the up counter is reseted with Hi-Z outputs, the EEPROM is active with outputs enabled, and the data from the EEPROM is asynchronously latched to the down counter. During state C both the up and down counters are released and begin counting. During state D the EEPROM goes into standby mode, and the output of the EEPROM goes into Hi-Z. State D defines the normal operation of the controller when the solenoids are driven. During state E the power fail is initiated, the up counter's value is latched to the output, and the EEPROM is active with the address being latched. During state F the data from the up counter is latched to the EEPROM and takes 5ms to write.

Voltage sensing circuits are necessary to trigger the start up and power fail. The MC34164 micropower undervoltage sensing circuits provide low voltage detection with a single pull up resistor. The output is low when the input voltage is less than 4.3V and the resistor pulls the output high when the input is above 4.3V. A voltage divider may be added to the input of the sensing circuit to alter the threshold value. For the power fail, a sensing circuit detects the voltage across the filter capacitor of the linear regulator. A voltage divider at the input changes the threshold

to 12V. The threshold was chosen to be sufficiently far the natural ripple of the filter

capacitor. This ensures that the power fail will not trigger during normal operation.
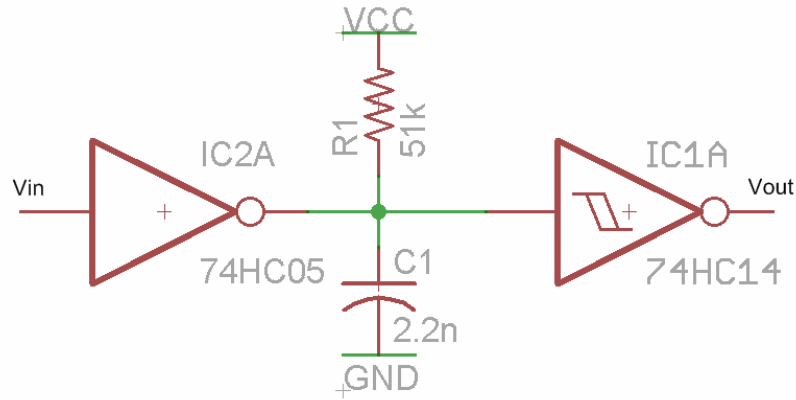

Figure 5: Delay Circuit

A 1st order charging RC circuit can achieve the necessary delay to achieve the

timing scheme for the controller. Figure 5 shows the circuit that implements this

delay. The 74HC05 is an open drain hex inverter. When the input is high the output of

the open drain inverter is pulled to ground. When the input is low the output is

floating and a pull-up resistor pulls the output high. Placing a capacitor between the

output and ground creates an RC charging circuit. The capacitor is shorted when the

input is high. The output of the open drain inverter exponentially charges to V_{CC}

when the input goes low.

$$V(t) = V_o \left(1 - e^{-\frac{t}{\tau}} \right) \tag{1}$$

The voltage across a charging capacitor is shown in (1) where $V_o = V_{CC}$, the

source, and $\tau = RC$, the time constant. The upper threshold voltage of the Schmitt

trigger is 2.5V and V_{CC} is 5V; therefore, $V_o = 5V$ and at 50μs $V(t) = 2.5V$. With

$R = 51kΩ$, to minimize DC current, the capacitance must be greater than 1.41nF. A
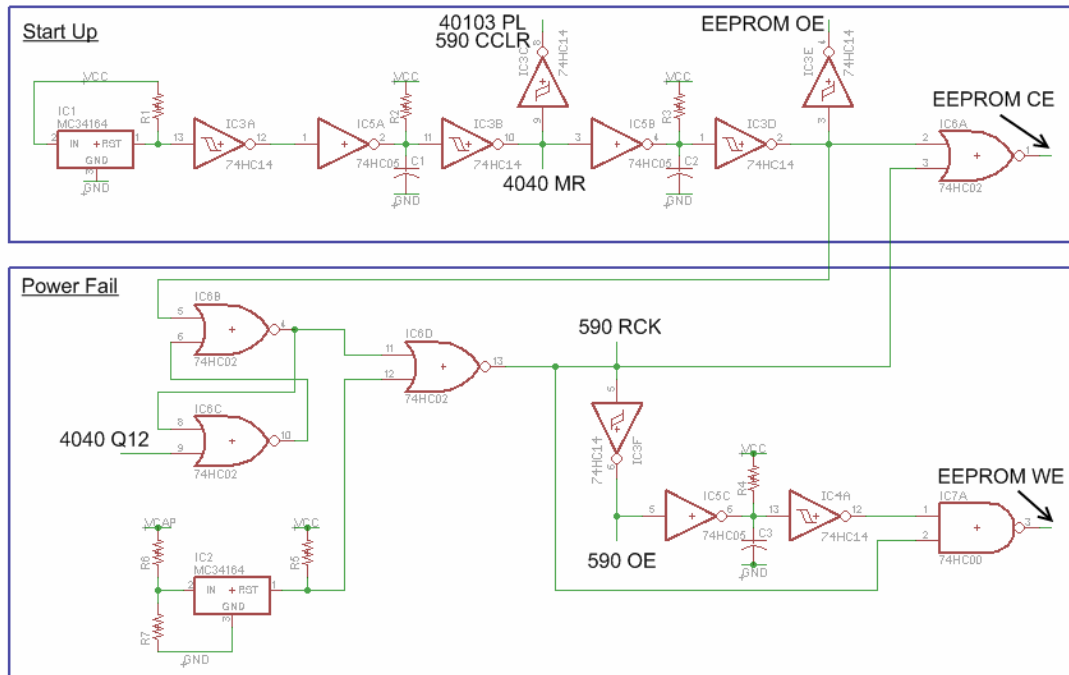
nominal capacitance of $C = 2.2nF$ was chosen.

Figure 6: Timing Circuit

The circuit shown in Figure 6 produces the timing diagram shown in Figure 4.

At start up the output of IC1 goes high when the sensing circuit detects a rail of 5V.

The open drain inverter needs a logic low to initiate the RC charging circuit; thus, an

inverter is needed between IC1 and IC5A. The EEPROM CE signal is triggered by a

NOR gate to allow the signal to go high then low as required by the timing diagram.

The NOR SR latch created by IC6B and IC6C ensure that a write cycle only

occurs after at least 30 seconds. The SR latch is reseted at start up while the Q12 pin

of the 74HC4040 is used to set the latch. The signal at Q12 divides the 60Hz clock by

2^{12} and has a period of 68.3 seconds. The signal goes high and sets the SR latch 34.2 seconds, half the period, after start up. The inverting output of the SR latch and the sensing circuit are fed into a NOR gate. The power fail sequence is initiated only when both inputs of IC6D go low. Power fail is initiated when IC2 detects that the filter capacitor voltage is under 12V which implies that power is removed and the capacitor is discharging. The NAND gate IC7A allows EEPROM WE to go low then high again after at least 50µs.

The valve solenoids require $24V_{rms}$ and draws at most $0.23A_{rms}$ for residential valves and $0.28A_{rms}$ for industrial valves. Designed for industrial specifications to incorporate both valve types in the controller. Each solenoid needs a switch to allow and block AC current to turn it on and off respectively. A triac, or triode for alternating current, is a bidirectional switch and turns on when DC current is applied to the gate terminal. The triac turns off at the end of each half cycle of the load current if no current is applied to the gate. Triacs may operate with positive gate voltage, 1st and 4th quadrant, or with negative gate voltage, 2nd and 3rd quadrant. Due to the internal construction of the triac the 4th quadrant requires greater gate current. However, for the ease of design the triac was designed to operate in the 1st and 4th quadrant with positive gate trigger voltage. The 2N6071B sensitive gate triacs were chosen because they have low gate trigger current and may be driven by CMOS logic gates. The 2N6071B can source up to $4A_{rms}$ which is more than enough to drive the valve solenoids.
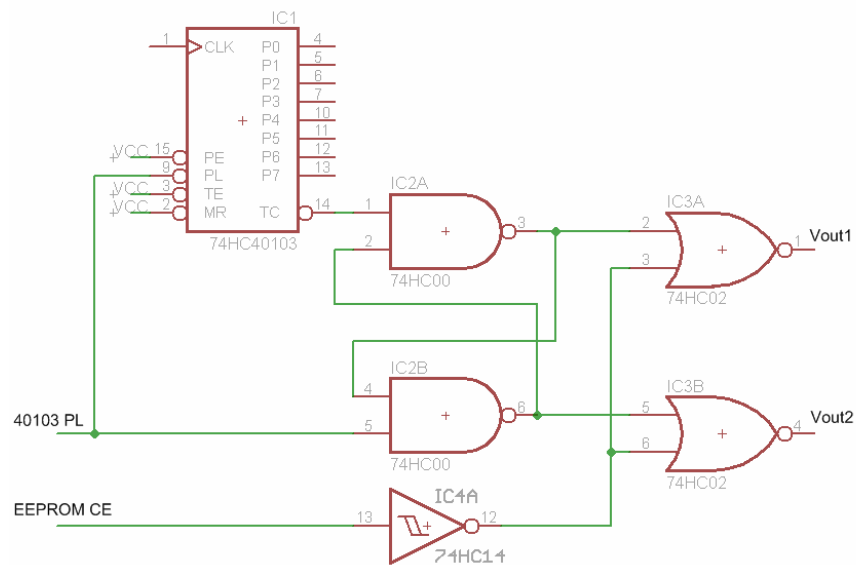
Figure 7: Driver Circuit

The down counter controls the switching of the valves. When the down counter reaches zero the TC output goes low for one clock cycle. A NAND SR latch detects this pulse. The 40103 PL signal resets the SR latch at start up and the down counter sets the latch at count zero; this effectively inverts the two outputs of the SR latch. The OR gates ensure that the controller only drives the triacs during normal operation, not during start up or power fail. This reduces the power demand of the regulator when the EEPROM is active. The EEPROM is in standby when CE is high, thus this signal may be used to trigger the triacs. The OR gates only drive the output high if both inputs are low. Therefore, the triacs are driven when the EEPROM is in standby, or CE is high. Initially V_{out1} is high and V_{out2} is low, but when the down counter reaches zero V_{out1} goes low and V_{out2} goes high.
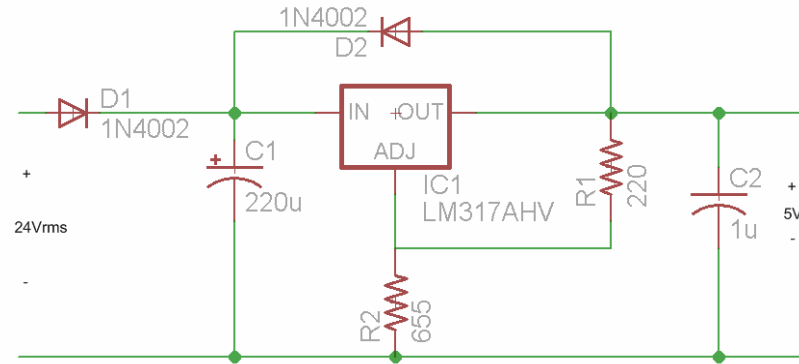
Figure 8: Power Supply

The power supply used to DC bias the digital logic is shown in Figure 8. The circuit consists of a half-wave rectifier, D_1 and C_1, and a linear voltage regulator, IC1. Assuming the voltage of the line may be ±20% of the nominal voltage, the maximum peak may be 40.8V. With a 5V output, the maximum input-output differential of the regulator could be 35.8V. The LM317AHV has a rated input-output differential of 60V, which is sufficient for this design. Using CMOS logic circuits reduces the power dissipated through the regulator by minimizing its load current. Resistors R_1 and R_2 adjust the output voltage of the regulator. An internal 1.25V reference voltage biases current through R_1, and this current flows through R_2 generating a voltage drop. The output voltage is approximated by (2).

$$V_{out} = 1.25\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 \qquad (2)$$

The I_{ADJ} current internally biases the 1.25V reference voltage and flows out of the adjustment terminal, with $I_{ADJ} = 46\mu A$. The voltage regulator requires a minimum

load current of 3.5mA to maintain regulation. Setting $R_1 = 220\Omega$ ensures a load

current of at least 5.7mA. Using (2), $R_2 = 655\Omega$ for an output voltage of 5V.

The power supply must supply the most current when the EEPROM is active

and this occurs at start up and power fail. During this time the EEPROM drawls

25mA and R_1 of the voltage regulator drawls 5.7mA. The remaining CMOS logic

biasing current ignored because they are in the micro-amps and the gate current of the

triacs ignored because they are disabled at this time. The approximation in (3) used to

calculate the required filter capacitor.

$$I = C\frac{\Delta V}{\Delta t} \tag{3}$$

In (3) ΔV is the ripple voltage, Δt is the period of the line signal, and I is the load

current. Arbitrary chose the ripple voltage at 10V to prevent the 12V triggering of the

power fail voltage sensing circuit. The period of a 60Hz signal is 16.7ms and the

maximum load current is 30.7mA. Using (3), the filter capacitor must be greater than

51.3μF. Using this capacitor value at power fail the voltage drops 3V after 5ms.

When power fail is triggered at 12V the voltage drops to 9V after the required time

for EEPROM writing. Thus the regulator can still power the digital logic during the

entire write sequence because the regulator needs the input to be at least 3V larger

than the output. The filter capacitor was chosen to be 220μF because electrolytic

capacitors have a limited lifespan. The capacitance begins to lower as the electrolyte

dissipates within the element. Using a larger capacitor increases the life of the device.

Capacitor C_2 provides addition filtering and insures stability. With this capacitor a

protection diode, D_2, is required to prevent the capacitor from discharging through the low current points of the regulator.

A well designed device should have overload and surge protection. Overload protection protects the electronics from current overload due to short circuiting. Current limiters, such as positive temperature coefficient (PTC) thermistors, protect against current overload. The resistance of the thermistor increases as the temperature increases. Heat is generated inside the PTC when power increases, and the PTC limits the power dissipation in the system by increasing its resistance and limiting the current to a low value. The advantage of using PTCs in overload protection over conventional fuses is that PTCs reset after the overload and do not need to be replaced. Surge protection protects the circuit from voltage spikes. Voltage clamping devices prevent voltage spikes from damaging the electronics. A metal oxide varistor (MOV) displays a nonlinear variable resistance that absorbs the over voltage surge by lowering its impedance. This clamps the voltage to a tolerable value for the electronics.

The maximum voltage, current, and temperature during normal operations must be taken into account when choosing protection devices. The normal operating current must be less then the maximum hold current of the PTC and the normal operating voltage must be less the maximum continuous voltage of the MOV. This prevents accidental triggering of the devices. Three PTCs are needed to protect the controller; one before the rectifier to protect the DC bias of the integrated circuits, and two in series with the triacs to protect them from shorting the outputs. The PTC

before the rectifier must have a maximum hold current larger than the nominal bias

current during start up or power fail. This was previously estimated at 30.7mA and

allowing for 20% error the maximum may approach 36.9mA. The littelfuse 60R010

provides over current limiting under 60V, sufficient for $24V_{rms}$, and has a maximum

hold of 60mA at 60°C. Since PTCs are temperature dependent, the maximum hold

current decreases as temperature increases. The PTC in series with the triacs must

have a maximum hold current larger than the holding current through the solenoids.

The maximum hold current through the solenoids is 0.28A and allowing for 20%

error the maximum is 0.336A. The littelfuse 60R065 provides over current limiting

under 60V, and has a maximum hold of 0.41A at 60°C. The MOV were chosen to

have a maximum continuous voltage greater than $24V_{rms}$ plus 20%. The littelfuse

V47ZA7P has a maximum continuous voltage of $30V_{rms}$.

V.   Construction

To build the controller, each section must be tested to ensure functionality. The blocks were divided into the driver, the frequency detector, the delay circuit, power supply, and the start up and power fail circuits. After testing these modules the controller may be integrated together.
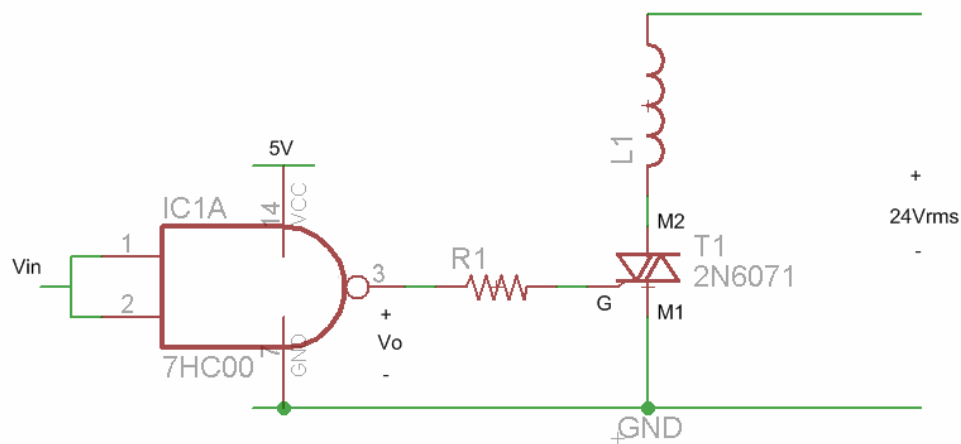

Figure 9: Triac Driver Test Circuit

The test circuit in Figure 9 demonstrates if a 74HC logic circuit can drive the triac and if the 2N6071 triac can trigger the valve solenoid. The valve solenoid, shown in Figure 10, is represented by the inductor L_1. When V_{in} is low, the output V_o goes high and produces gate current for the triac. The triac then conducts and allows current to flow through the solenoid. There is no gate current when V_{in} is high. Thus,

the trac does not conduct and no current flows through the solenoid. Used a $120V_{rms}$

to $24V_{rms}$ transformer to represent the AC voltage line.

Figure 10: Picture of Valve Solenoid

R_1 (Ω)	V_o (V)	$V_{R1 (V)}$	I_G (mA)	V_G (V)	V_{AC} (V_{rms})	V_{M2-M1} (V_{rms})	V_L (V_{rms})
1000	4.74	4.51	4.51	0.225	26.22	0.792	25.68
900	4.72	4.47	4.9667	0.24	26.23	0.791	25.7
800	4.68	4.43	5.5375	0.263	26.22	0.789	25.7
700	4.65	4.36	6.2286	0.289	26.23	0.792	25.97
600	4.61	4.28	7.1334	0.32	26.21	0.792	25.65
500	4.54	4.19	8.38	0.348	26.23	0.79	25.684
400	4.46	4.06	10.15	0.382	26.23	0.784	25.69

Table I: Gate Resistor Sweep of Driver Test Circuit

To test the driver circuit, the gate resistor was swept. Table I shows the test

results of the driver circuit with the gate resistor between 1kΩ and 400Ω. Above 1kΩ

the triac failed to turn on because the driver circuit could not produce enough gate

current to trigger the triac. As the gate resistance decreased, the gate current

increased. Must look at the temperature extremes to determine the necessary gate

resistor for the controller. As the temperature decreases the necessary gate trigger

current increases. At 0°C the minimum gate trigger current is 5.5mA and the gate

trigger voltage is 1.75V. The gate resistor must be less than 590Ω to achieve this, and

a nominal resistance of 560Ω was chosen.

Originally the frequency detector shown in Figure 3 was built without a series

current limiting resistor and a capacitor with a large capacitance that provided low

impedance and little attenuation. The $24V_{rms}$ line drove too much current through the

protection diodes of the Schmitt trigger and damaged the integrated circuit. The

frequency detector does not need to preserve the phase of the line; therefore, an

attenuating capacitor may be used to attenuate the line to a $5V_{pp}$ sine wave. Adding a

resistor in series would prevent damaging by limiting the current through the

protection diodes. First a 10kΩ resistor was used to limit the current but this produced

unwanted phase noise in the square wave and the 74HC4040 did not divide the

frequency correctly. Replacing the current limiting resistor to 1kΩ fixed this. Figure

11 shows the input 60Hz $24V_{rms}$ line voltage and Figure 12 shows the attenuated

signal with offset. The attenuated signal has more noise associated with it, but the

hysteresis of the Schmitt trigger prevents unwanted triggering. Figure 13 shows the

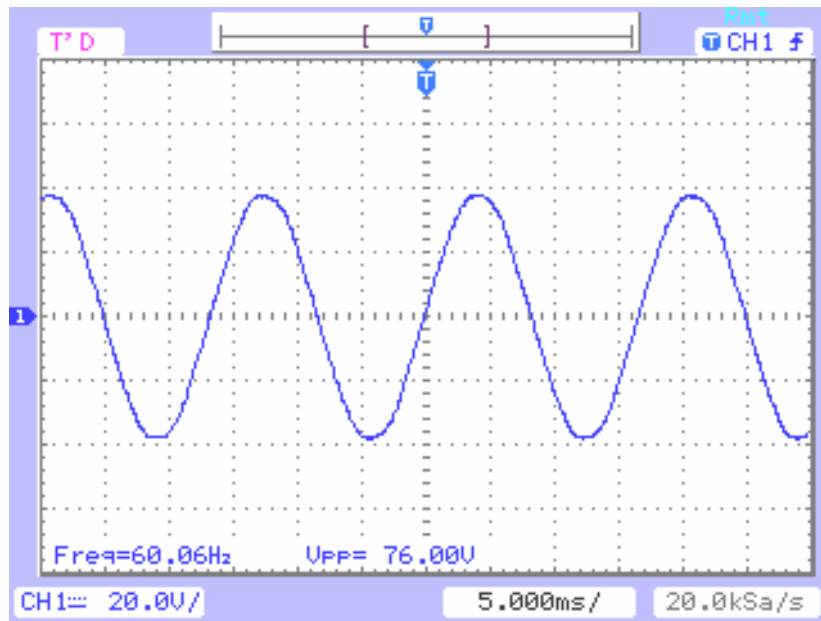appropriate 60Hz square wave after the Schmitt trigger suitable for the clock.

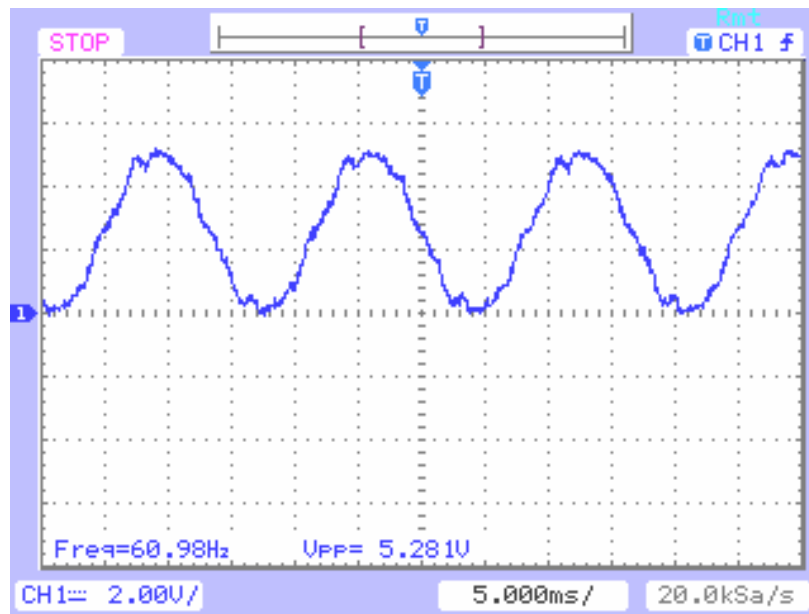**Figure 11: Waveform of 60Hz 24V$_{rms}$ Voltage Line**

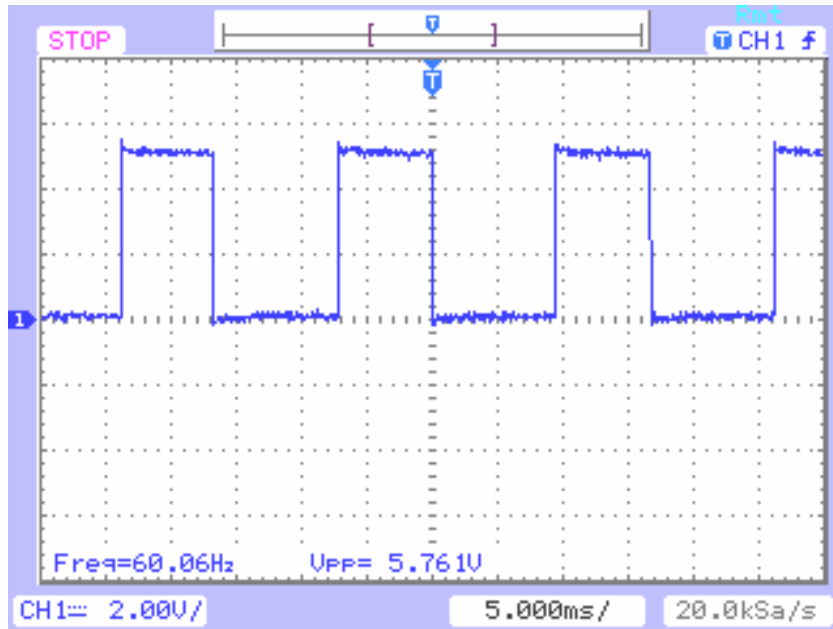**Figure 12: Attenuated Waveform with 5.281V$_{pp}$ and 2.5V Offset**

Figure 13: 60Hz Square Wave with 5.761V$_{pp}$

The delay circuit in Figure 5 was constructed and tested. Figure 14 shows the testing waveforms of the delay circuit with channel 1 as the input and channel 2 as the output. The input is a 3kHz square wave and the output is delayed for 84.23μs after the falling edge. As discussed in the design section, the delay is only after the falling edge and not during the rising edge. The actual capacitance was 2.37nF and the actual resistance was 50.3kΩ. This correlates to a theoretical time delay of 82.6μs and a percent error of 2.0% according to (3).

$$\% \; error = \frac{\exp erimental - theoretical}{theoretical} x100\% \qquad (3)$$

When testing this circuit the waveforms had distortion in logic level high and the circuit was drawing more current than specified in datasheet. Since the other Schmitt triggers were not being used the inputs were in unknown state. They were probably

oscillating since CMOS logic only drawls current during switching. Grounding the unused gates solved the problem.
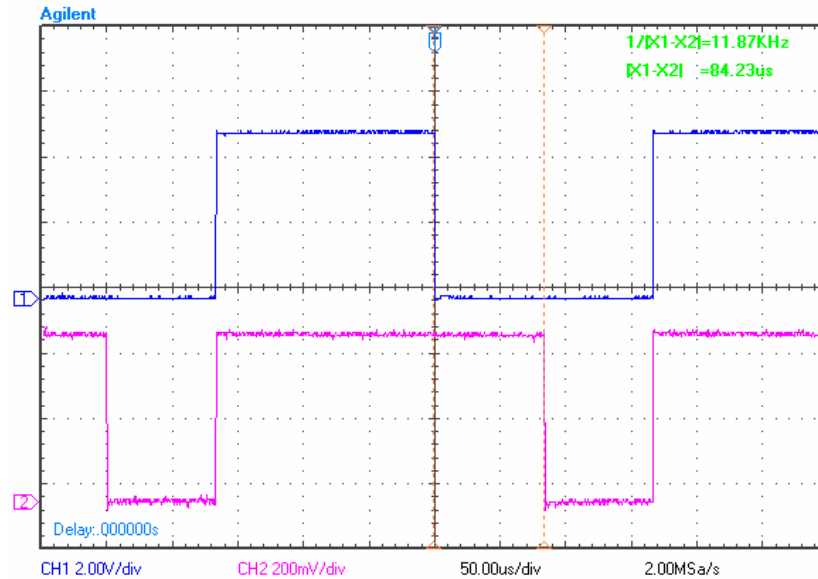

Figure 14: Delay Circuit Waveforms

Next tested the start up circuit with the power supply, the frequency divider, and the down counter. Constructed the power supply designed in Figure 8 with $R_1 = 220\Omega$ and $R_2 = 651\Omega$ and resulted with $V_{out} = 5.02V$. The frequency detector was integrated with the 74HC4040 frequency divider. The start up circuit in Figure 6 controlled the 74HC40103 down counter with a pre-set input register. Manually changing the input register altered the down counting time which confirms start up operation. The power fail circuit in Figure 6 was constructed to test the write sequence of the EEPROM. Needed to design the voltage divider of IC2 of the power

fail circuit. Chose $R_7 = 42\text{k}\Omega$ because the MC34164 triggers at 4.3V and at this voltage the current through the resistor is 102μA. This is much greater than the input quiescent current of 12μA and thus a voltage divider is possible. Choosing $R_6 = 24.1\text{k}\Omega$ creates a sensing threshold of 12.1V. The power fail circuit successfully wrote data to the EEPROM. Setting the EEPROM to read demonstrated that the data could be recovered after power was removed.

VI.   Integration

Integration consists of putting the separate tested blocks together to form a functioning system. First the start up circuit and the down counter was connected to the EEPROM to determine if the down counter could read from the EEPROM. This was done by pre-programming the EEPROM separately. Then used the start up circuit to set the EEPROM to the read cycle. Afterwards the up counter was integrated with the down counter and EEPROM to form an 8-bit bus. Then connected the power fail circuit to the EEPROM. Initially the controller was tested without the triacs and the driver circuit. The SR latch after the down counter was probed to determine if it triggered at the appropriate time. The timing circuit divided the total run time in half within clock frequency resolution. Also, running the controller for less then 30 seconds inhibited the write cycle as to specifications.

The driver circuit and triacs were added when the timing circuit was successfully tested. However, the triacs were connected incorrectly and when powered the $24V_{rms}$ line was applied to the 5V rails. Consequentially, all the integrated circuits powered by the 5V rails were damaged. Not only were the integrated circuits damaged but also the transformer. The transformer is rated to 1670mA. Therefore, the transformer must have been shorted. This incident demonstrates the importance of using protection circuits. Surge and overload protection devices prevent electronic damage due to excess voltage and current respectively. All the integrated circuits had to be replaced. To test the circuit without

the 24V$_{rms}$ line a function generator was used to provide the 60 Hz 5V$_{pp}$ clock and the

linear regulator was driven by a DC power supply.
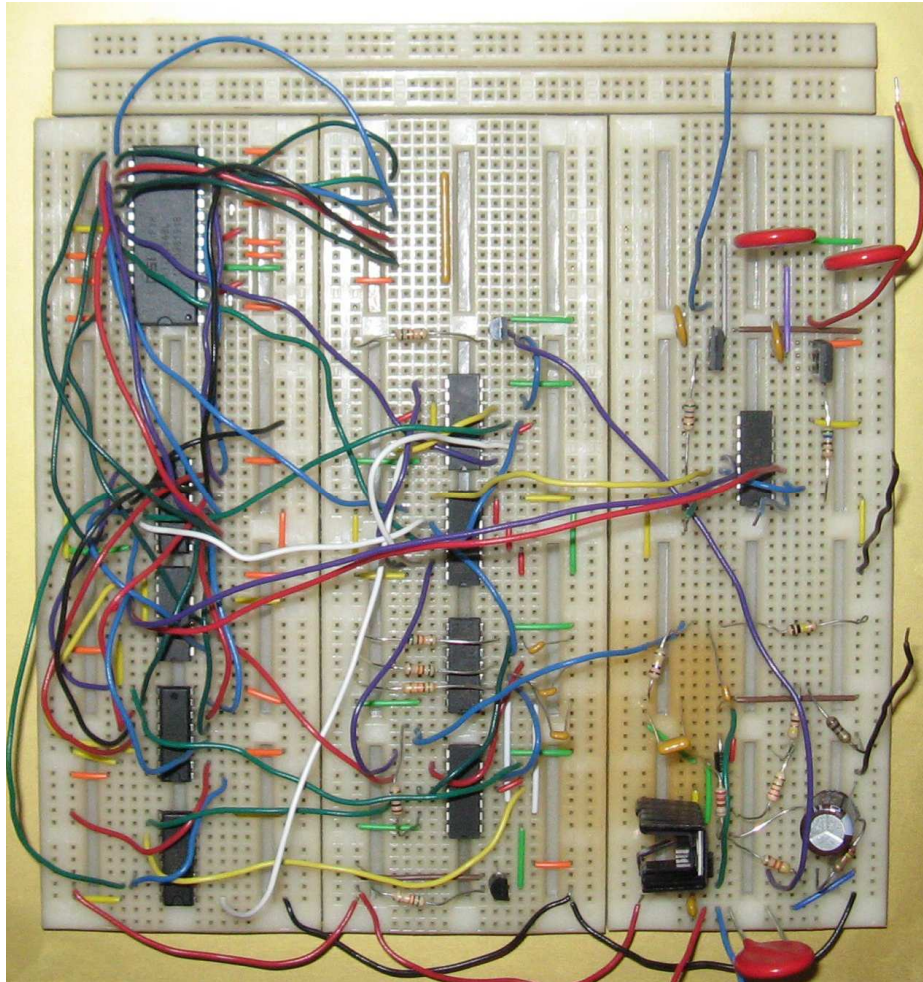
Figure 15: Breadboard Prototype

After determining the timing circuit still worked and getting a new

transformer, the triacs and driver circuit were added. Also the PTCs and MOVs were

added as a precaution. Figure 15 shows the breadboard prototype of the controller

without the solenoid loads. To attach the solenoids, one end of both was connected to

the 24V$_{rms}$ line while the other ends were connected to the M2 pin of the triacs. The

timing circuit and driver circuit successfully drove the triacs and solenoids. The two triacs successfully switched between the two solenoids when triggered. Table II demonstrates the solenoid switching time for various run times. The switching time should be half of the programmed time. To test, the controller was run for the programmed time period. Then the controller was reseted and the time of switching was recorded. The discrete clock period cause the quantization error in the switching time. The period of the down counter clock is 17.1 seconds. Therefore, the switching time is half the program time with a maximum error of -17.1 seconds. This quantization error becomes insignificant at larger controller running times.

Programmed Time (min:sec)	Switching Time (min:sec)
2:00	0:58
4:00	1:48
6:00	2:59
8:00	3:48
10:00	4:54
15:00	7:25
20:00	9:46

Table II: Solenoid Switching Time for Various Running Times

With the AC source of $26.22V_{rms}$ the solenoid drew $0.19A_{rms}$ and had a voltage drop of $25.5V_{rms}$. Therefore the solenoids require 4.84W from the line. The gate current through the traic is 7.59mA. With the sensitive gate triac, a gate current two orders of magnitude smaller than the solenoid load current can control the irrigation valve. The linear voltage regulator drives 15.2mA of current during normal operation. Only 1.91mA biases the timing circuit because 5.7mA flows through the adjustment voltage divider and 7.79 mA drives the gate of the triac. Figure 16 shows the ripple voltage of the filter capacitor of the half-wave rectifier. This is the ripple

during normal operation and it ripples between 35.32V and 34.25V. With a mean

voltage of 34.79V the average voltage drop across the regulator is 29.79V. With a

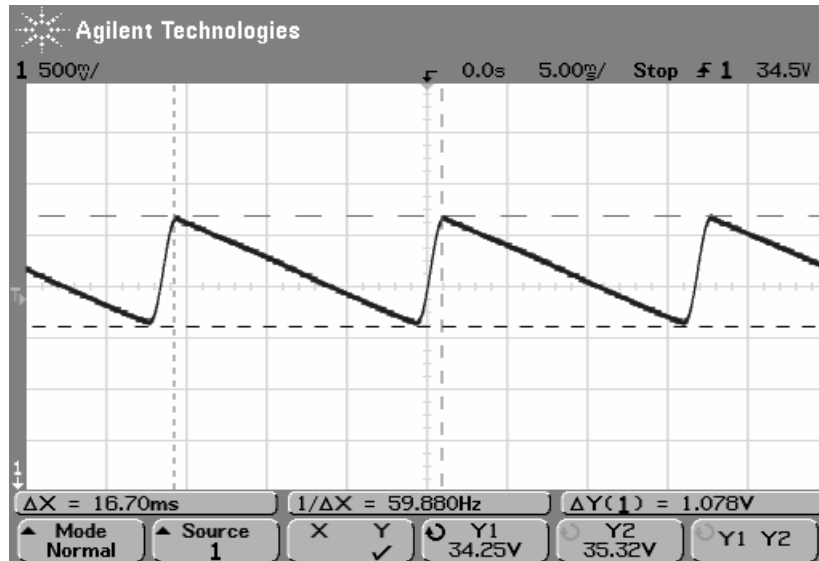load current of 15.2mA the average power dissipation across the regulator is 453mW.

Figure 16: Filter Capacitor Voltage Ripple during Normal Operation

More power was dissipated across the regulator than anticipated. This is due

to the triac gate current and the adjustment voltage divider current of the regulator.

Increasing the triac gate resistor would lower the load current, but the triac may not

trigger at 0°C. Also, increasing the adjustment voltage divider resistors would

decrease the load current, but the voltage regulator would no longer be guaranteed its

minimum load current for proper operation. There is a trade off between guaranteed

operation and efficiency. After running the controller for 20 minutes, with a 1cm by

2cm heat sink, the voltage regulator was not hot to the touch. The voltage regulator

may need a larger heat sink for 2 hours of operation. To make the controller more

efficient a transformer may be added to the voltage line to step down the voltage. This

would reduce the power dissipation across the linear regulator. However, this would increase the size of the controller package. Using a transformer would only be necessary if the required heat sink for 2 hours of operation is larger than transformer. Since this is unlikely, this design omitted the transformer. With a working prototype and schematic, a printed circuit board can be routed for a commercial product.

VII. Conclusion

The intelligent irrigation zone splitter allows easy expansion for already existing irrigation controllers. The zone splitter controller uses an existing valve zone line to control two separate valves creating a new irrigation zone. This allows expansion without disturbing the already built foundation. The controller splits the total watering time in half between the two zones. The controller uses the previous watering time to calculate the next watering time. This allows the controller to be programmed to different watering periods.

The controller uses counters to control the zones. An up counter measures the total watering time, whereas a down counter controls the triac switching. An EEPROM, a non-volatile memory, stores and remembers the total watering time. At start up the up counter starts to count, the EEPROM latches its data to the down counter, and the down counter starts to count. At power fail the total watering time measured by the up counter is stored to the EEPROM. The frequency of the down counter is twice the frequency of the up counter; therefore, the down counter splits the previous total watering time in half. The controller uses the $24V_{rms}$ 60Hz line to power the device, set the clock, and drive the valve solenoids. This allows the controller to be self sufficient.

The built intelligent irrigation zone splitter prototype was built as a system. The controller was split into different building blocks each requiring testing and troubleshooting. The building blocks could be integrated together when each

individual block was tested and worked per specification. This ensured minimum troubleshooting when the system is built.

The timing circuit divided the total watering time in half within allowed quantization error due to the slow clock frequencies. The quantization error becomes minimal as the total watering time increases. The power supply was not very efficient because there was no transformer to step down the line voltage. This was justified because adding a transformer would substantially increase the controller size. The intelligent irrigation zone splitter prototype demonstrated that the circuit can divide the total watering time in half and be programmable to drive the valve solenoids for different time periods.

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Appendix A – Schematic
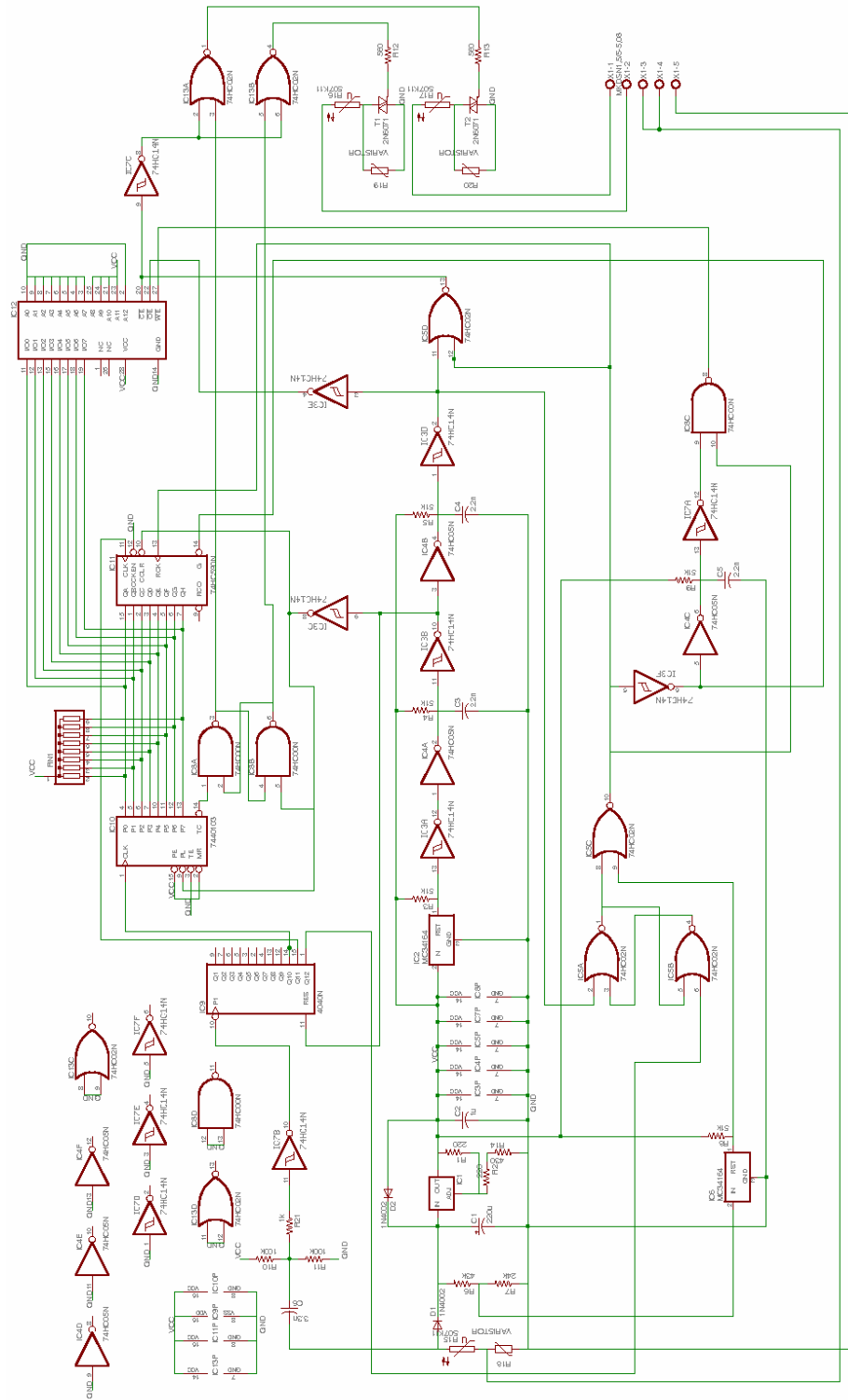
Appendix B – Parts List and Cost

Quantity	Part	Cost Per Part	Total Cost
1	LM317HVT	$0.54	$0.54
1	SN74HC590AN	$0.66	$0.66
1	CD74HC40103E	$0.81	$0.81
1	CD74HC4040E	$0.70	$0.70
2	MC34164P-5G	$0.70	$1.40
2	2N6071B	$0.52	$1.04
1	CAT28C64BL12	$4.26	$4.26
1	74HC00N	$0.25	$0.25
2	74HC02N	$0.25	$0.50
2	74HC14N	$0.25	$0.50
1	M74HC05	$0.36	$0.36
1	60R010XU	$0.26	$0.26
2	60R065XU	$0.28	$0.56
3	V47ZA7P	$0.31	$0.93
2	1N4002	$0.07	$0.14
1	Resistor Array (SIL)	$0.48	$0.48
1	Electrolytic Capacitor	$0.62	$0.62
5	Multi-Layer Capacitor	$0.31	$1.55
3	1% Resistors	$0.14	$0.42
10	5% Resistors	$0.10	$1.00
1	Transformer	$9.50	$9.50
		Total	$26.48