

ANALYSIS AND DESIGN OF MULTIPHASE MULTI-  
INTERLEAVE DC-DC CONVERTER WITH INPUT-OUTPUT  
BYPASS CAPACITOR

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Master of Science in Electrical Engineering

by

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## APPROVAL PAGE

TITLE: ANALYSIS AND DESIGN OF MULTIPHASE MULTI-  
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# **ABSTRACT**

## **ANALYSIS AND DESIGN OF MULTIPHASE MULTI-INTERLEAVE DC-DC CONVERTER WITH INPUT-OUTPUT BYPASS CAPACITOR**

The power requirements for the microprocessor have been increasing as per Moore's Law. According to International Technology Roadmap (ITRS), the Voltage Regulator Module (VRM) for the microprocessor will be 200 W(with 1V, 200A output) in 2010. With the VRMs topology of synchronous buck, serious technical challenges such as small duty cycle, high switching frequencies, and higher current demands, contribute to decreased power density and increased cost.

This thesis proposes a Multiphase Multi-Interleave Buck topology to solve the technical challenges of powering future microprocessors. The critical design parameter values are selected using the theoretical design equations and calculations. The design is simulated in OrCAD Pspice to evaluate the performance criteria of the VRM. A prototype of four-phase Multiphase Multi-Interleave Buck Converter is constructed. The critical performance parameters of the prototype are tested and measured. The thesis concludes with the performance of the prototype as compared with the performance of the design simulation.

## **ACKNOWLEDGEMENTS**

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## **Chapter 1    Introduction**

### **1.1    Power Electronics**

*“Power electronics is the technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form” [1] or it may be defined as*

*“The applications of the solid state electronics with power, electronics and control”.*

It combines power, electronics and control. The control deals with the steady state and dynamic characteristics of closed loop systems. The power deals with the static and rotating power equipment for the generation, transmission and distribution of electric energy. The electronics deal with the solid state devices and circuits for signal processing to meet the desired control objectives [2]. Power electronics refers to control and conversion of electrical power by power semiconductor devices wherein these devices operate as switches [3].

Advent of silicon-controlled rectifiers, abbreviated as SCRs, led to the development of Power Electronics. Prior to the introduction of SCRs, mercury-arc rectifiers were used for controlling electrical power, but such rectifier circuits were part of industrial electronics and the scope for applications of mercury-arc rectifiers was limited. Once the SCRs were available, the application area spread to many fields such as drives, power supplies, aviation electronics, high frequency inverters, and this originated the new field of power electronics. In modern systems the conversion is performed with semiconductor switching devices such as diodes, thyristors, transistors, IGBTs and GTOs. In contrast to electronic systems concerned with transmission and processing of signals and data, in power electronics substantial amounts of electrical energy are

processed. The most typical power electronics devices can be found in many consumer electronic devices, e.g., television sets, personal computers, battery chargers, etc. The power range is typically from tens of watts to several hundred watts. Power electronics provides power conversion process where goals are to reduce the power loss and increase energy efficiency with reduction in size, weight and the overall cost of the unit.

## 1.2 Types of Power Electronics Circuits

In general, power electronics circuits can be classified into six types:

- Diode Rectifier
- AC-DC Converter (Controlled Rectifier)
- AC-AC Converter (AC Voltage Controller)
- DC-AC Converter (Inverter)
- DC-DC Converter (DC Chopper)
- Static Switch

### 1.2.1 Diode Rectifier

A diode rectifier circuit converts AC voltage into a fixed DC voltage. The input voltage to the rectifier could be either single phase or three phase.

### 1.2.2 AC-DC Converter

A single phase AC-DC converter is the circuit with two naturally commutated thyristors, which converts AC power to DC power. The average of the output voltage can be controlled by varying the conduction time of thyristors or firing angle. The input could be single or three phase source. These converters are also known as Controlled Rectifiers.

### 1.2.3 AC-AC Converter

These converters are used to obtain a variable AC output voltage from a fixed AC source and a single phase converter with a bidirectional switch such as Triac. The output voltage is controlled by varying the conduction time or firing delay angle of the switch. This type of converter is also known as AC Voltage Controller.

### 1.2.4 DC-AC Converter

A DC-AC converter is also known as an Inverter. An inverter is an electronic circuit that converts DC to AC. Inverters are used in a wide range of applications, from Uninterruptable Power Supply (UPS), Adjustable Speed Drives (ASDs) to large electric utility applications that transport bulk power. The inverter is so named because it performs the opposite function of a rectifier.

### 1.2.5 DC-DC Converter

DC-DC converters are power electronics circuits that convert a fixed voltage DC source on to a variable DC output. A DC converter can be considered as the DC equivalent to an AC transformer with a continuously variable turns ratio. Like a transformer, it can be used to step down or step up a DC voltage source.

### 1.2.6 Static Switch

The power devices can be operated as static switches or contactors, the supply to these could be either AC or DC, and the switches are called AC Static Switches or DC Switches consecutively.

Electronic switch-mode DC to DC converters convert one DC voltage level to another by storing the input energy temporarily and then releasing that energy to the output at a different voltage. The storage may be in either magnetic components like



inductors, transformers or capacitors. This conversion method is more power efficient, often 80% to 98%, than linear voltage regulation, which dissipates unwanted power as heat. This efficiency is beneficial to increasing the running time of battery operated devices. Drawbacks of switching converters include cost, complexity and electronic noise (EMI / RFI). There are two types of DC-DC converters: Non-Isolated and Isolated DC-DC converters. Non-Isolated topology is a transformer-less technique in which the input and output share a common ground. Non-Isolated topologies are typically used in board level power distribution and Isolated topologies are used in off-line power supply.

Some examples of transformer-less converter topologies include:

- Buck Converter
- Boost Converter
- Buck-Boost Converter
- Cuk Converter
- Single Ended Primary Inductor Converter (SEPIC)

For the isolated or transformer connected converters, the common topologies are:

- Forward Converter
- Push-pull Converter
- Flyback Converter
- Half-Bridge Converter
- Full-Bridge Converter

## 1.2.7 Non-Isolated DC-DC Converters

### 1.2.8 Buck Converter

A buck converter is a step-down DC to DC converter. It is a switched-mode power supply that uses two switches; a transistor and a diode, an inductor and a capacitor.

The output voltage function for buck converter is

$$V_o = DV_{IN} \quad \text{Equation 1.1}$$

Where D = Duty cycle

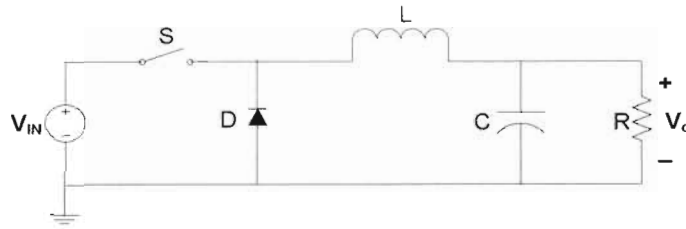


Figure 1.1 Buck Converter

The above equation is valid only when the buck converter operates in Continuous Conduction Mode (CCM). CCM occurs when  $i_L > 0$ .

### 1.2.9 Boost Converter

A boost converter, step-up converter is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching mode power supply, called SMPS, containing at least two semiconductor switches, a diode and a transistor, and at least one energy storage element. Filters made of inductor and capacitor combinations are often added to a converter's output to improve performance. The output voltage function for this converter is

$$V_o = \frac{V_{IN}}{1-D} \quad (\text{CCM}) \quad \text{Equation 1.2}$$

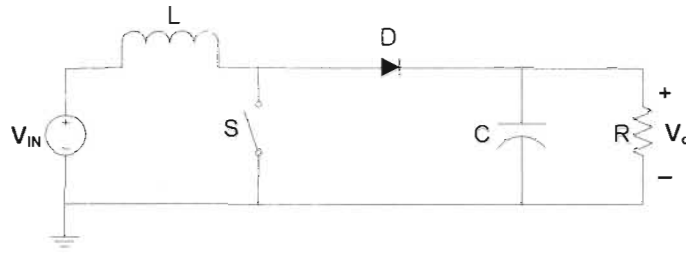


Figure 1.2 Boost Converter

### 1.2.10 Buck-Boost Converter

The buck-boost converter is a type of DC-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. It is a switch mode power supply with a similar circuit topology to the boost converter and the buck converter. The output voltage is adjustable based on the duty cycle of the switching transistor. The polarity of the output voltage is opposite to that of the input voltage. The output function buck-boost converter is given by

$$V_o = -\left(\frac{D}{1-D}\right)V_{IN} \quad (\text{CCM}) \quad \text{Equation 1.3}$$

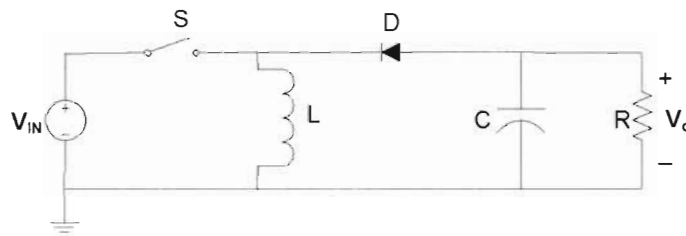


Figure 1.3 Buck Boost Converter

### 1.2.11 Cuk Converter

The cuk converter is a type of DC-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude, with an opposite polarity. It uses a capacitor as its main energy-storage component, unlike most other types of converters which use an inductor. Cuk converter offers the benefits over

buck-boost converter in terms of low ripple input and output current. The output voltage function is

$$V_o = -\left(\frac{D}{1-D}\right)V_{IN} \quad (\text{CCM}) \quad \text{Equation 1.4}$$

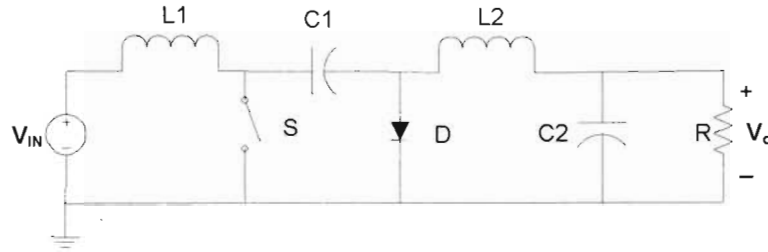


Figure 1.4 Cuk Converter

### 1.2.12 Single Ended Primary Inductor Converter (SEPIC)

A SEPIC is a DC-DC converter which allows the output voltage to be greater than, less than, or equal to the input voltage. The output voltage of the SEPIC is controlled by the duty cycle of the control transistor. The greatest advantage of a SEPIC over the buck-boost converter is a non-inverted output i.e. positive voltage. Output voltage is given by a function

$$V_o = \left(\frac{D}{1-D}\right)V_{IN} \quad (\text{CCM}) \quad \text{Equation 1.5}$$

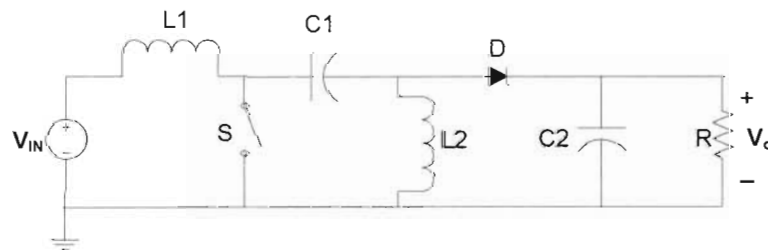


Figure 1.5 SEPIC

### 1.2.13 Isolated DC-DC Converters

### 1.2.14 Push-Pull Converter

A push-pull converter is a type of DC to DC converter that uses a transformer to change the voltage of a DC power supply. The transformer turns ratio is arbitrary but

fixed; however, in many circuit implementations the duty cycle of the switching action can be varied to affect a range of voltage ratios. The primary advantages of push-pull converters are their simplicity and ability to scale up to high power throughput, earning them a place in industrial DC power applications. Push-Pull topology in Figure 1.6 is used in up to 300 W power level and it is a very attractive choice for telephony industry power supplies where the maximum DC input voltage is specified as only 60 V. The output voltage is given by

$$V_O = 2V_{IN} \left( \frac{N_s}{N_p} \right) D \quad (\text{CCM}) \quad \text{Equation 1.6}$$

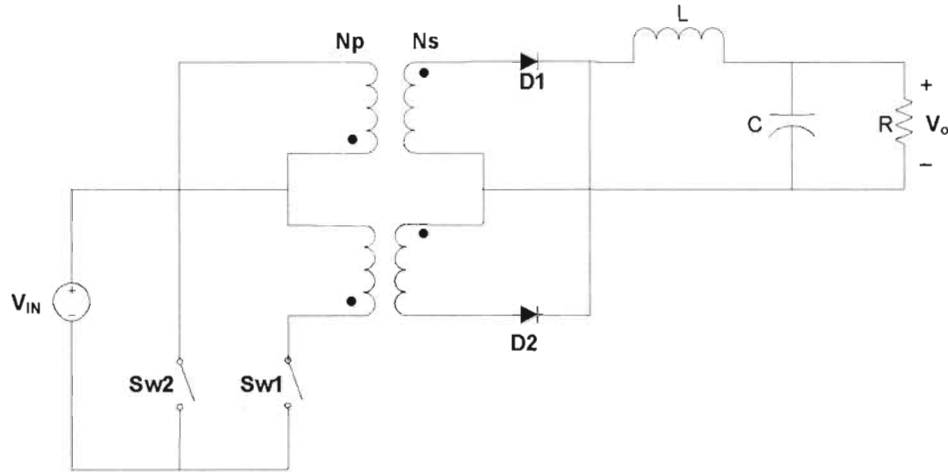


Figure 1.6 Push Pull Converter

### 1.2.15 Forward Converter

Single switch forward topology is more economical and required less space than push-pull. It is very popular for low power applications and most widely used for output power under 200 W. The output voltage is given by the following relation

$$V_O = V_{IN} \left( \frac{N_s}{N_p} \right) D \quad (\text{CCM}) \quad \text{Equation 1.7}$$

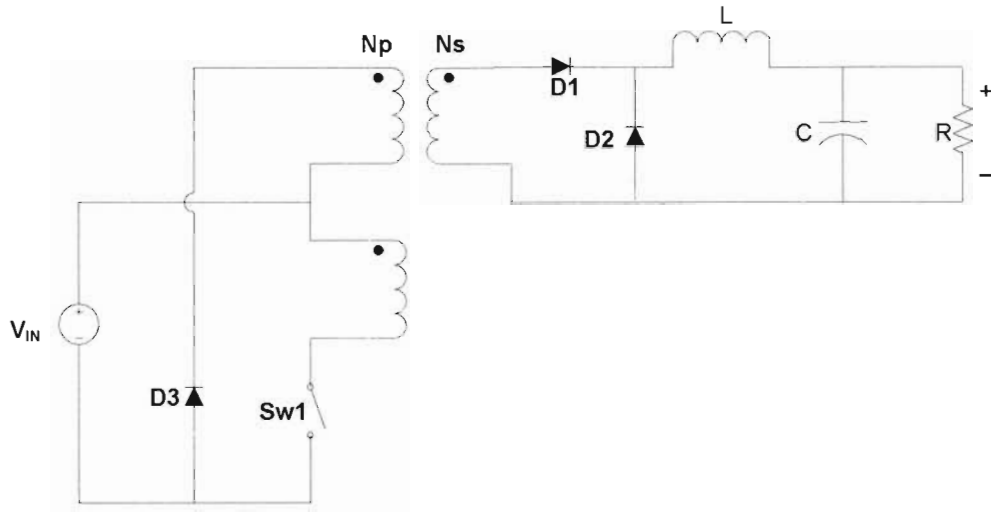


Figure 1.7 Forward Converter

### 1.2.16 Flyback Converter

The flyback converter is a DC to DC converter with a galvanic isolation between the input and the output. More precisely, the flyback converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of isolation. Flyback topology in Figure 1.8 has fewer parts compared to forward and push-pull but suffers from higher output ripple due to the absence of output inductor. Output voltage relation is

$$V_o = V_{IN} \left( \frac{N_s}{N_p} \right) \left( \frac{D}{1-D} \right) \quad (\text{CCM}) \quad \text{Equation 1.8}$$

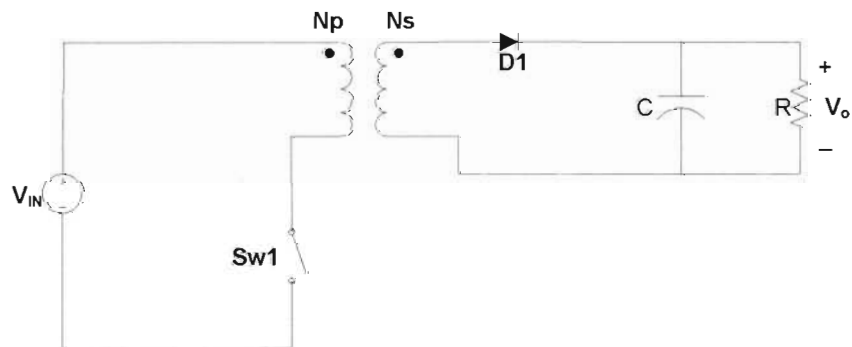


Figure 1.8 Flyback Converter

### 1.2.17 Half-Bridge Converter

Half-bridge converter is the most friendly solution for direct off-line switch mode power supplies because of the reduced voltage stress on the primary switching devices. The half bridge converter is similar to the push pull converter, but a centre tapped primary is not required. The reversal of the magnetic field is achieved by reversing the direction of the primary winding current flow. This type of converter is found in high power applications. The output voltage is given by

$$V_o = V_{IN} \left( \frac{N_s}{N_p} \right) D \quad \text{CCM} \quad \text{Equation 1.9}$$

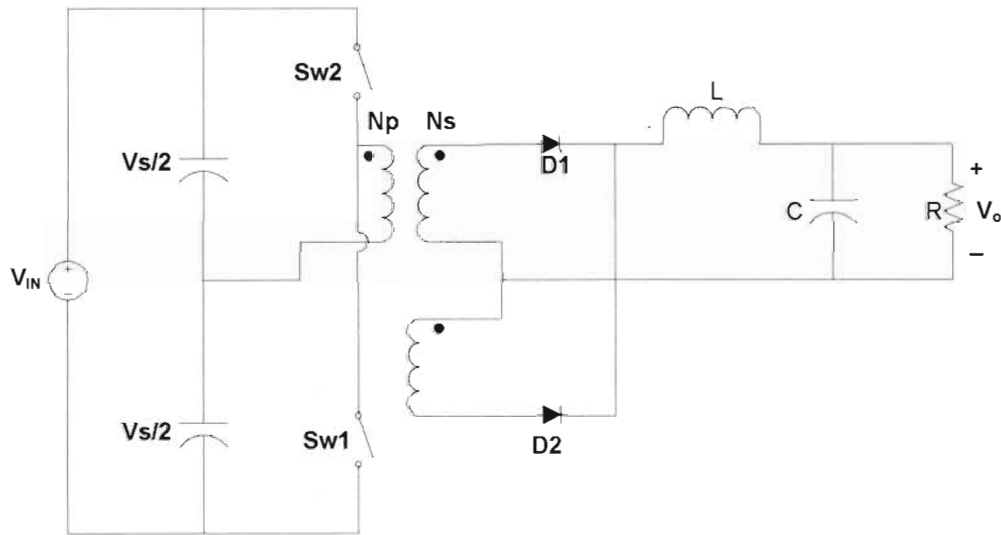


Figure 1.9 Half Bridge Converter

### 1.2.18 Full-Bridge Converter

Comparing full-bridge converter in Figure 1.10 to the half-bridge, the two controlled switches in half-bridge are replaced by the input capacitors. The output voltage function of full-bridge converter is given by

$$V_o = 2V_{IN} \left( \frac{N_s}{N_p} \right) D \quad \text{CCM} \quad \text{Equation 1.10}$$

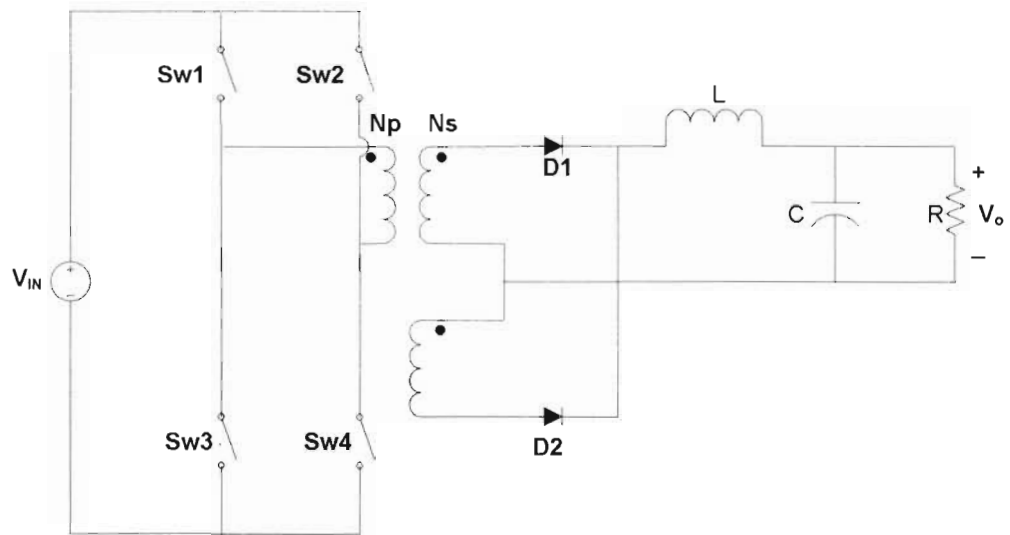


Figure 1.10 Full Bridge Converter



## Chapter 2 Voltage Regulator Modules

### 2.1 Definition

*“A voltage regulator module (VRM) is an installable module that senses a computer's microprocessor voltage requirements and ensures that the correct voltage is maintained” [4].*

The number of transistors on a chip has been increasing exponentially and according to Moore's Law it doubles every two years, see Figure 2.1 [5]. Based on Intel's data, transistor's count in a microprocessor will increase to 1 billion in 2010. In terms of speed, future microprocessors are expected to run at 15 GHz [6]. The increase in both the number of transistors and the speed of future microprocessors poses a major challenge in powering their operation. It has been known widely that to decrease the power consumption, microprocessor's supply voltage for the next generations of microprocessors must be as low as possible.

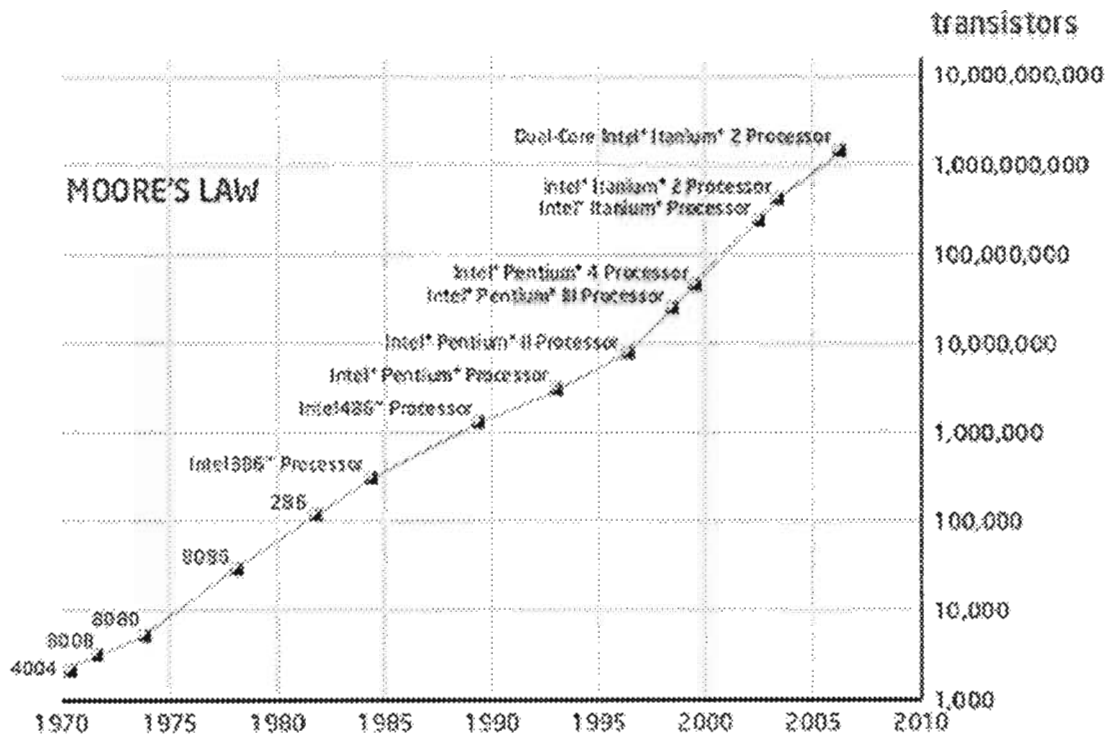


Figure 2.1 Moore's Law and Intel Processors

However, technical conflicts arise when the power supply to these microprocessors, widely known as Voltage Regulator Module (VRM) is operated at voltage below 1V. In 2010, future microprocessors are expected to draw current 150 A with 0.8 V supply voltage as shown in Figures 2.2 and 2.3 [7]. As the number of transistors increases per Moore's Law, the power requirements for the microprocessor also increase. International Technology Roadmap for Semiconductors (ITRS) predicts allowable maximum power requirements will increase as seen in Figure 2.4 [7] and there is a necessity to reduce the power consumption of the microprocessor. Based on these figures, the design of future VRMs will face some serious technical challenges since it will involve low output voltage like 1 V, high output current, fast transient response, high efficiency, high power density and low cost.

### ITRS Trends for Power Supply Currents

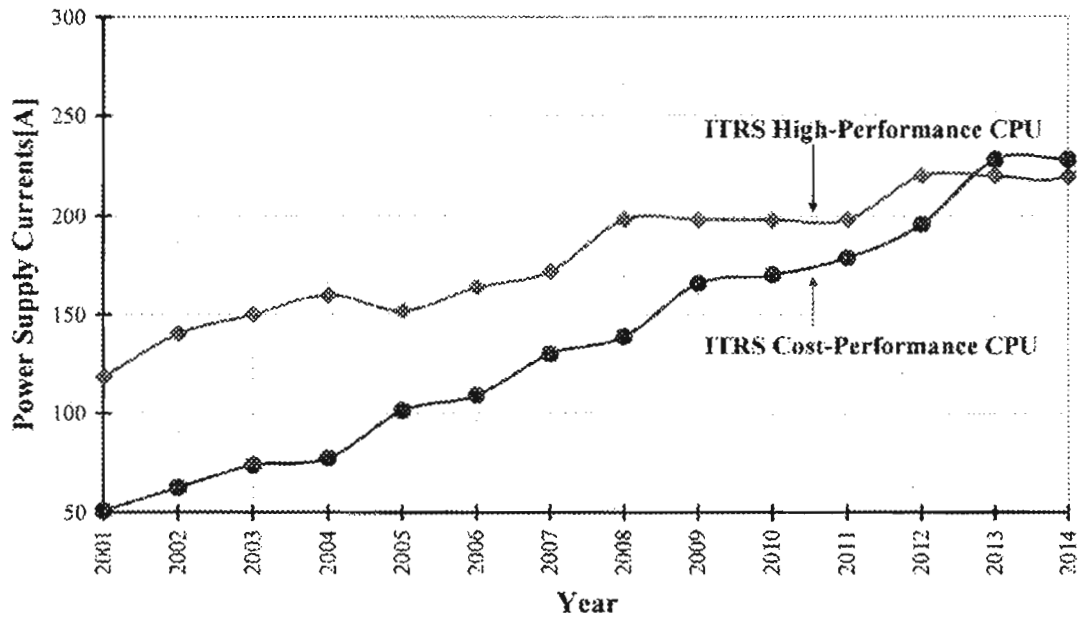


Figure 2.2 Calculated Values for Power Supply Currents

### ITRS Trends for Power Supply Voltages

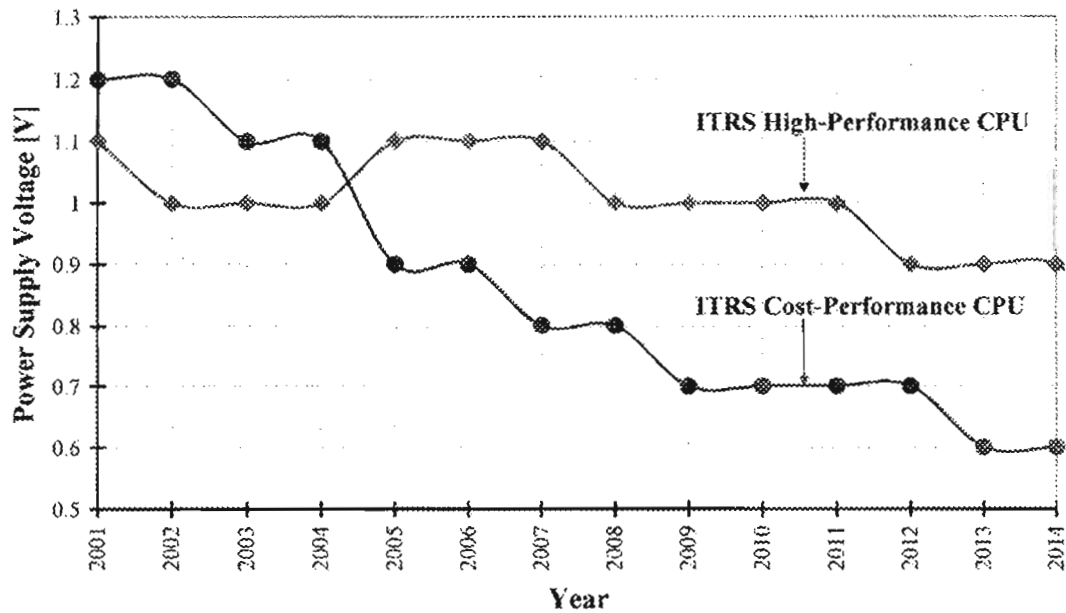


Figure 2.3 Roadmap Trend for Power Supply Voltage

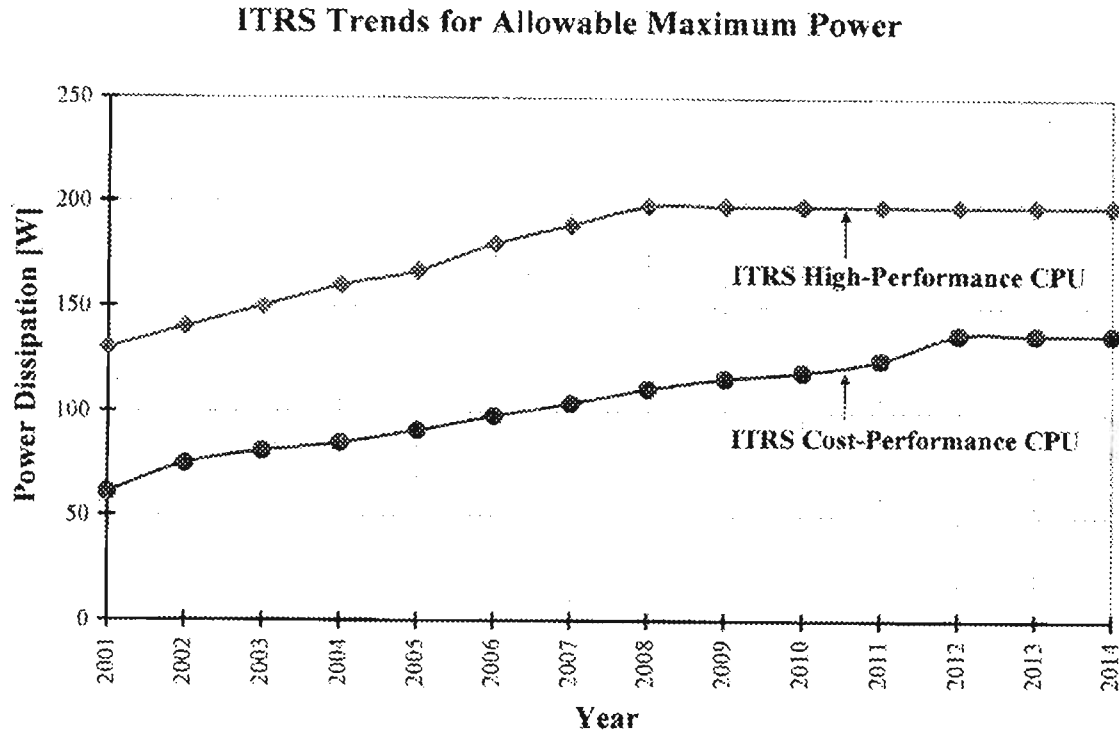


Figure 2.4 Roadmap by ITRS for Future Power Requirements

The very basic stage of voltage regulator modules is the Synchronous Buck Converter. Even with complex new topologies being developed nowadays, the VRMs still use the synchronous buck converter as a fundamental unit due to efficiency that it offers. The following section will explore the design and operation of synchronous buck converter which is important to understand the proposed new VRM topologies as discussed later.

## 2.2 Synchronous Buck Converter

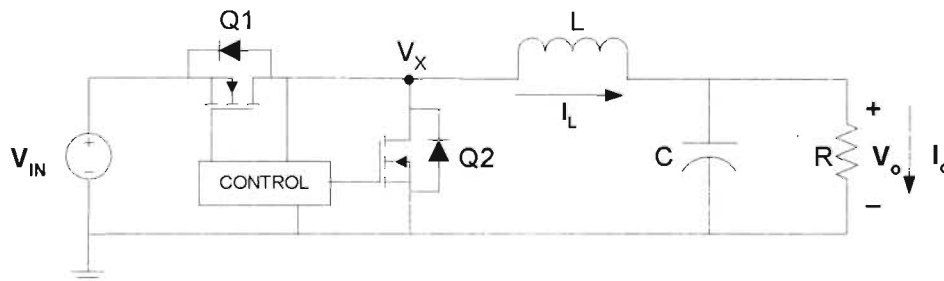


Figure 2.5 Synchronous Buck Converter

The difference between a regular buck converter and a synchronous buck converter is that the freewheeling diode in the regular buck converter is replaced by another switch [8]. This replacement basically enhances the efficiency of the buck converter since diode's forward voltage drop is one of the reasons of poor efficiency of the converter at low voltage and high current output. In addition to the switch, usually another Schottky diode is placed in parallel in order to further reduce the reverse recovery loss and to provide the dead time required to avoid a dead short due to simultaneous conduction of both switches.

In terms of its operation, synchronous buck works the same way as that of the basic buck converter. Referring to Figure 2.5, first switch  $Q_1$  turns on and the current flows through it to charge inductor  $L$ . After some time  $Q_1$  turns off and  $Q_2$  gets turned on. Now the inductor will discharge through or freewheel  $Q_2$ . To prevent the circuit from input current spike, there is always a delay between turning on and off of two switches and that delay is called the dead time. A Schottky or a fast reverse recovery diode connected in parallel with  $Q_2$  serves the purpose of conducting during that dead time with less forward voltage drop before the next cycle starts. The following section discusses the design of a synchronous buck converter.

### 2.2.1 Design of a Synchronous Buck Converter

Ideal duty cycle is given by expression [9].

$$D = \frac{V_o}{V_{IN}} \quad \text{Equation 2.1}$$

According to the steady state requirement, which states that Voltage-Second product of the inductor remains the same during ON time and OFF time [9]:

$$\frac{(V_{IN} - V_o)DT}{L} = \frac{V_o(1-D)T}{L} \quad \text{Equation 2.2}$$

However all real world components have some losses, so taking losses at switches and inductor into consideration the above equation becomes:

$$\frac{(V_{IN} - I_o R_{Q1} - I_o R_L - V_o)DT_s}{L} = \frac{(V_o + I_o R_{Q2} + I_o R_L)(1-D)T_s}{L} \quad \text{Equation 2.3}$$

Solving for D yields:

$$\Rightarrow D = \frac{V_o + I_o(R_{Q2} + R_L)}{V_{IN} + I_o(R_{Q2} - R_{Q1})} \quad \text{Equation 2.4}$$

where

$R_{Q1}$  is the ON resistance of upper switch Q1 [ $\Omega$ ]

$R_{Q2}$  is the ON resistance of lower switch Q2 [ $\Omega$ ]

$R_L$  is the dc resistance of inductor which is also known as DCR [ $\Omega$ ]

$T_s$  is the input switching period [Secs]

$I_o$  is the output current [A]

Inductance can be calculated by using volt-second balance during OFF time [9]:

$$L = \frac{V_o(1-D)T_s}{\Delta I_L} \quad \text{[H]} \quad \text{Equation 2.5}$$

or

$$\Rightarrow L = \frac{V_o(1-D)}{\Delta I_L f_s} \quad \text{[H]} \quad \text{Equation 2.6}$$

where  $f_s$  is the switching frequency in Hz.

The output capacitor of the Buck Converter, which is used to reduce the output voltage ripple, is given by [9]:

$$C = \frac{V_o(1-D)}{8Lf_s^2\Delta V_o} \quad [\text{F}] \quad \text{Equation 2.7}$$

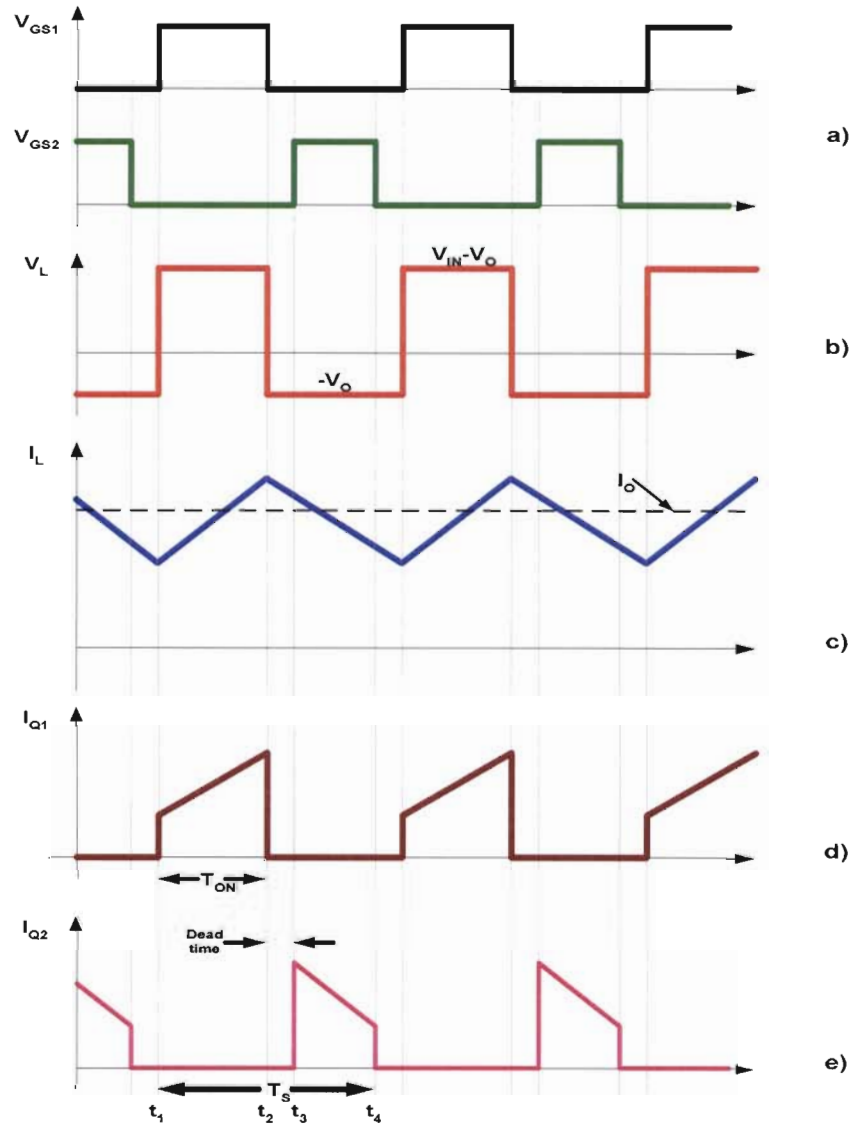


Figure 2.6 Waveforms of Synchronous Buck Converter: (a) Gate Drive Signals for Q1 and Q2, (b) Inductor Voltage (c) Inductor Current (d) Current through Q1 (e) Current through Q2

Figure 2.6 illustrates the critical waveforms as explained previously. It is clear from the figure that when the signal is applied at the gate of switch  $Q_1$ , the inductor charges linearly and when the signal is applied at the gate of  $Q_2$  the inductor discharges linearly. In real world no component is loss-less. Every inductor and capacitor has direct

current resistance DCR and equivalent series resistance ESR respectively. Therefore in designing a converter we have to take into account these losses as well.

The switch used in synchronous buck converter is typically the type that we call MOSFETs. MOSFETs are typically associated with switching loss, conduction loss, gate drive loss and body diode loss [2],[8], and can be written as:

$$P_{MOSFET} = P_{SW} + P_{COND} + P_{GD} + P_{BD} \quad [W] \quad \text{Equation 2.8}$$

For MOSFET  $Q_1$ :

The switching loss  $P_{SW}$  is

$$P_{SW} = \frac{1}{2} I_O V_{IN} (t_R + t_F) f_s \quad [W] \quad \text{Equation 2.9}$$

where  $t_R$  and  $t_F$  are rise and fall times of the drain-source voltage  $V_{DS}$  and drain current  $I_D$

The conduction loss  $P_{COND}$  is

$$P_{COND} = I_O^2 R_{DS(ON),Q1} D \quad [W] \quad \text{Equation 2.10}$$

where  $R_{DS(ON)}$  is the drain to source resistance of the switch  $Q_1$  in on-state  $[\Omega]$

The body diode loss  $P_{BD}$  can be calculated as

$$P_{BD} = t_{DEADTIME} V_F I_O f_s + Q_{RR} V_{IN} f_s \quad [W] \quad \text{Equation 2.11}$$

where  $Q_{RR}$  is the diode reverse recovery charge  $[C]$

The gate drive loss  $P_{GD}$  is approximated as

$$P_{GD} = Q_G V_{GS} f_s \quad [W] \quad \text{Equation 2.12}$$

where

$Q_G$  is the total gate charge of the switch  $[C]$

$V_{GS}$  is the gate to source voltage of the switch  $[V]$



No body diode loss should be considered with  $Q_1$ . Basically body diode loss is the conduction and reverse recovery loss in the diode when it freewheels during the dead time. There is no current to freewheel  $Q_1$  which means there would not be any body diode loss. Hence, the total loss  $P_{Q1}$  at  $Q_1$  is the sum of all above losses except for the body diode loss and can be written cumulatively:

$$P_{Q1} = \frac{1}{2} I_O V_{IN} (t_R + t_F) f_S + I_O^2 R_{DS(ON),Q1} D + Q_G V_{GS} f_S \quad [W] \quad \text{Equation 2.13}$$

Similarly for MOSFET  $Q_2$ , the following equations give the expressions for switching losses, conduction losses, body diode losses and gate drive losses respectively.

$$P_{SW} = \frac{1}{2} I_O V_{IN} (t_R + t_F) f_S \quad [W] \quad \text{Equation 2.14}$$

$$P_{COND} = I_O^2 R_{RD(ON),Q2} (1 - D) \quad [W] \quad \text{Equation 2.15}$$

$$P_{BD} = t_{DEADTIME} V_F I_O f_S + Q_{RR} V_{IN} f_S \quad [W] \quad \text{Equation 2.16}$$

$$P_{GD} = Q_G V_{GS} f_S \quad [W] \quad \text{Equation 2.17}$$

The total power loss  $P_{Q2}$  for switch  $Q_2$  is given by:

$$P_{Q2} = \frac{1}{2} I_O V_{IN} (t_R + t_F) f_S + I_O^2 R_{DS(ON),Q2} (1 - D) + Q_G V_{GS} f_S + t_{DEADTIME} V_{IN} I_O f_S + Q_{RR} V_{IN} f_S \quad [W] \quad \text{Equation 2.18}$$

So total loss  $P_{LOSS}$  in a circuit would be the sum of all these losses represented in equation 2.19.

$$P_{LOSS} = P_{Q1} + P_{Q2} + P_L + P_C \quad [W] \quad \text{Equation 2.19}$$

where  $P_L$  is a loss in inductor, which is

$$P_L = I_O^2 R_L \quad [W] \quad \text{Equation 2.20}$$

and  $P_C$  is a loss in capacitor, which is

$$P_C = \Delta I_L^2 R_C \quad [\text{W}] \quad \text{Equation 2.21}$$

where  $R_C$  is the equivalent series resistance of the capacitor  $[\Omega]$

Efficiency of the synchronous buck converter can be calculated as

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad \text{Equation 2.22}$$

where  $P_{OUT}$  is the power at output.

### 2.3 Issues with a Single Synchronous Buck for VRM

The low output voltage and high output current, requirements of the future microprocessors, make the synchronous buck topology a less ideal solution to power the microprocessors.

Low output voltage requirement is a setback in terms of duty cycle. In case of 12 V input voltage VRM to 1 V output voltage, according to equation 2.1, this topology suffers very small duty cycle and that is below 10%. This increases turn-off loss on the top switch and conduction loss on the bottom switch.

Quality of output voltage is of extreme importance for efficiency purposes. Quality is linked with output voltage ripple. To decrease the output voltage ripple in a synchronous buck, switching frequency is increased. This increase in switching frequency results in the switching, gate drive and body diode losses which are discussed in section 2.2. These all losses are directly proportional to switching frequency.

More efficient, smaller and power dense VRM is need of the time. One of the major draw backs of conventional or synchronous buck topology is that it operates at

lower frequency. Low operating frequency results in higher output voltage ripple. To overcome this problem of voltage ripple, higher filter inductance is used, which limits the transient response and it translates to limiting energy transfer speed. In order to meet the microprocessor requirements regarding output voltage ripple, huge output filter capacitors are needed which reduce the voltage ripple as well as help in reducing the voltage spike during the transient. These large sized capacitors would increase the size of the module and thereby make it impractical.

Capacitance can be reduced by increasing the current slew rate which is possible by using smaller filter inductances. However small inductances result in large current ripples in the circuit's steady state operation. The large current ripples generate steady state voltage ripples at the VRM output capacitor. The steady state output voltage ripples can be so large that they are comparable with transient voltage spikes. It is not only harmful action for the top switch due to larger turn off loss, but also for the bottom switch due to larger conduction loss.

As a result these technical conflicts do not only increase the costs and sacrifice the power density, but also make it very difficult to meet the power requirements of future microprocessors before the technical conflicts are resolved. In recent years, new converter topologies have been proposed to solve the technical conflicts discussed above.

## 2.4 Multiphase Voltage Regulator Modules

As discussed in the previous section, power management related issues become much more critical for future microprocessors and much more difficult to handle. To meet future microprocessor's specifications, high efficiency, high power density, fast

transient VRMs are required. To achieve this target, the following technological challenges should be addressed:

- Advanced VRM topologies to accommodate for high efficiency, high power density and fast transient response for low voltage, high current applications.
- Efficient synchronous rectification that incorporates new driving means or topologies to eliminate the body diode loss for high frequency operation.
- Innovative integrated magnetics for low core losses, low winding losses and easy manufacturability for high efficiency and high power density.
- Optimization of multiphase VRM that provides a methodology for determining the appropriate number of channels and value of output inductance for the optimal operation of VRMs.
- Advanced packaging technology to minimize parasitics for high frequency operation.

The fundamental limitation of the conventional single-phase buck converter is the tradeoff of efficiency and switching frequency. Output ripple and dynamic response improve with increased switching frequency. The physical size and value of the filter inductor and capacitors become smaller at higher switching frequencies. There is, however, a practical limitation to the switching frequency: switching losses increase with frequency, and resulting efficiency tends to be lower. The multiphase buck topology offers a solution to this conundrum. The fundamental frequency is effectively multiplied by the number of phases used, improving transient response. Other advantages of this solution include reduced input and output capacitor RMS currents and reduced EMI filtering requirements; decreased PCB size; better thermal performance.

As mentioned before, most of the multiphase VRMs today still employ the synchronous buck topology. In the following section, variations of synchronous buck topologies currently under investigation will be discussed.

#### 2.4.1 Multiphase and Multiphase Multi-Interleave Buck Converters

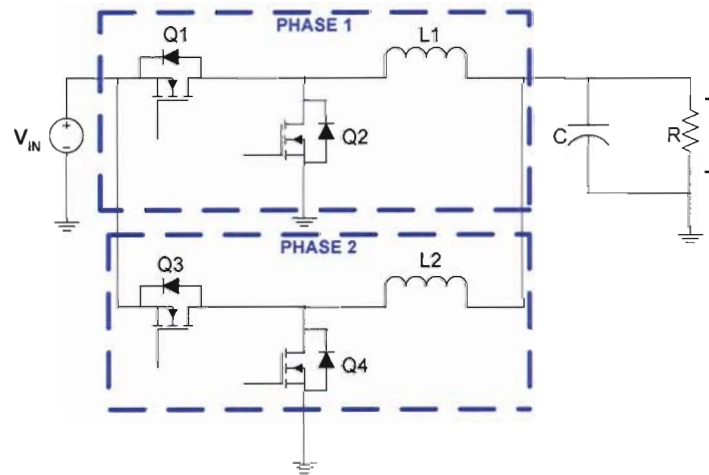


Figure 2.7 Multiphase Synchronous Buck VRM

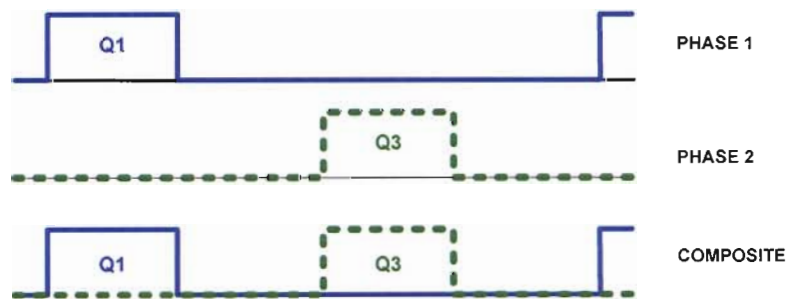


Figure 2.8 Gate Drive Signals for Multiphase Buck

In this section, the 2-phase buck operation will be discussed and how it can be extended to the optimized number of phases. Figure 2.7 shows the basic multiphase buck converter consisting of two buck converters in parallel. Each box with the dashed lines in Figure 2.7 represents the individual phase of VRM. Each phase is equal to none other than one synchronous buck converter. When two or more synchronous buck converters

are put in parallel, they may form a multiphase converter. To be called a Multiphase Converter, each buck has a switching control signal with phase difference of  $360^\circ/N$  where  $N$  is the phase number. So in case of the two phases, each phase control signal is shifted from each other by  $180^\circ$  as shown in Figure 2.8. In case of four phases, control signal for each phase is shifted from each other by  $90^\circ$  degrees and so on.

In the multiphase buck converter, duty cycle  $D$  is the ratio of the output voltage  $V_O$  and input voltage  $V_{IN}$  just like that in a regular buck converter. However, the main benefit of multiphase is the current ripple cancellation effect which enables the use of the small inductance to both improve transient response and minimize the output capacitance.

Multiphase converter combines all phase shifted inductor currents from individual channel or phase, and therefore greatly reduces the total current ripple flowing into the output capacitor. With the current ripple reduction, the output voltage ripples are also greatly reduced which enables the use of very small inductances in each phase to improve the transient response requirement. The reduced output ripple voltage in turn allows for more room for voltage variations during load transient because the ripple voltage will consume a smaller portion of the total voltage tolerance budget. Consequently, multiphasing helps to improve the load transient performance and minimize the output capacitance.

The multiphase buck increases the total output current frequency. The output current frequency is the multiple of the number of phases times the switching frequency of each buck converter, i.e.  $f_{Total} = f \cdot N$ . This provides another benefit of multiphase since the higher the output frequency the less filtering effort needed, further reducing the amount of output capacitance.

To do an interleaving of multiphase buck, there must be at least a minimum of two phases in a module and at least two modules. In this converter, the interleaving is done not only between the phases in one module but also between the modules. A multiphase interleaving buck topology greatly reduces the current ripple to the output capacitors. This in turn greatly reduces the steady state output voltage ripple, making it possible to use very small inductance in VRMs to improve the transient response. Interleaving VRMs with small inductances reduce both the steady state voltage ripples and the transient voltage spikes, so that a much smaller output capacitance can be used to meet the steady state and transient voltage requirements. As a result, the power density of the VRMs can be significantly improved. Moreover, interleaving buck converter makes the thermal dissipation more evenly distributed. Studies show that in high current application, the overall cost of the converter can be reduced using this technology [3]. Multiphase multi-interleaved converter is further discussed in Chapter 3.

#### 2.4.2 Multiphase Clamp Coupled-Buck Converter

As indicated previously, future microprocessor will operate at lower voltage. To the VRMs, this implies the decrease in the nominal duty cycle. To combat this problem, a multiphase topology called the Active Clamp Couple-Buck Converter is designed specifically to solve the extremely small duty ratio problem. Other benefits of this topology include recovery of leakage energy, clamped device voltage and reduced input filter. Until now experiments show that circuits based on this topology significantly improve the VRM efficiency.

The key feature of this topology is that it employs an inductor coupling into the synchronous buck converter, hence extending the extremely small duty ratio. Figure 2.9 shows the schematic of tapped-inductor buck converter.

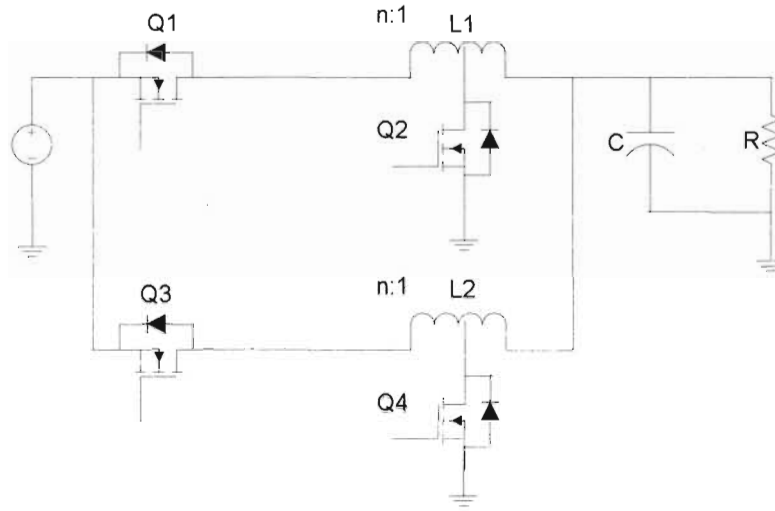


Figure 2.9 Multiphase Tapped-Inductor Buck Converter

According to its DC voltage gain shown in equation

$$M = \frac{V_o}{V_{IN}} = \frac{D}{D + n(1 - D)} \quad \text{Equation 2.23}$$

the duty ratio would extend significantly by increasing the turn ratio of the coupled output inductor. The optimal turn ratio can be decided by the transient response. To obtain a symmetrical transient response, the slope of the averaged inductor current during step down should equal to the slope during step up. Since these slopes change with the turn ratio, the optimal turn ratio can be determined according to the identical slopes during transients.

With an increased duty ratio, the turn off of top switches can be reduced significantly. In the tapped inductor buck, the turn off current is two times lower than in the buck converter. It is noted however, that the leakage inductance always exhibits



between the two windings of coupled inductors. Usually the leakage energy is dissipated and a voltage spike appears across the top switch.

Thus the voltage stress for top switches need to be doubled and the 30 V MOSFETs, which are widely used in the buck VRM, cannot be used. Conventional snubber circuits could be used to reduce this voltage spike. However, this implies additional components for each channel. For multiphase topologies, this will significantly increase the cost and the complexity. Therefore, the conventional way to solve the leakage current is not desirable. Simpler solutions are needed to solve the large voltage spike caused by the leakage inductance. This forms the base for an improved topology called the Active Clamp Coupled Buck Converter.

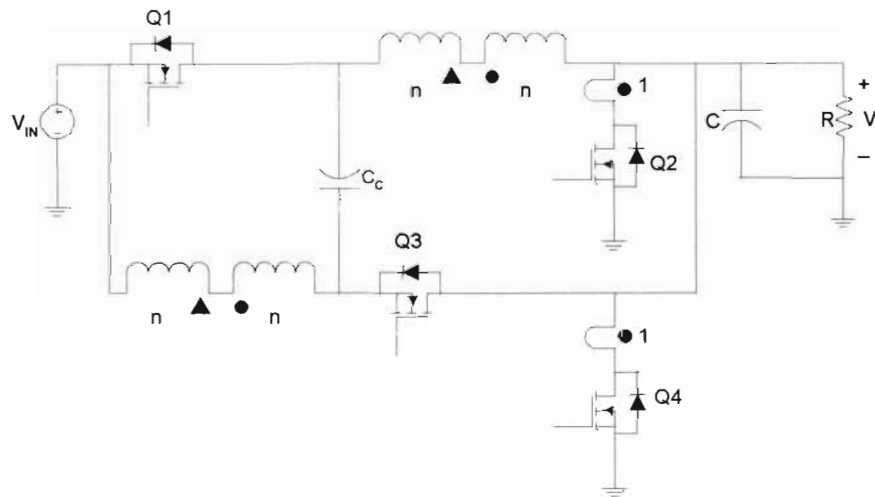


Figure 2.10 Active Clamp Coupled Buck Converter

This topology shown in Figure 2.10 enables the use of a larger duty ratio with a clamped and coupled structure. Therefore one can recover the leakage energy and clamp the voltage spike across the device. It has four operation stages in a half way cycle, which corresponds to the buck mode, leakage energy recovery mode, freewheel mode and leakage current reset mode. Another half switching cycle has the same operation stages.

According to the steady state operation waveforms, the DC voltage gain of the active clamp couple-buck converter can be obtained as shown in the following equation:

$$M = \frac{V_o}{V_{IN}} = \frac{D}{D + n} \quad \text{Equation 2.24}$$

The duty cycle can be extended by increasing the turn ratio of the coupled output. It has been experimentally proven that active clamp couple-buck VRM has more than 3% higher efficiency than the synchronous buck VRM, operating at 300 kHz [11].

### 2.4.3 Multiphase Phase-Shift Buck VRM

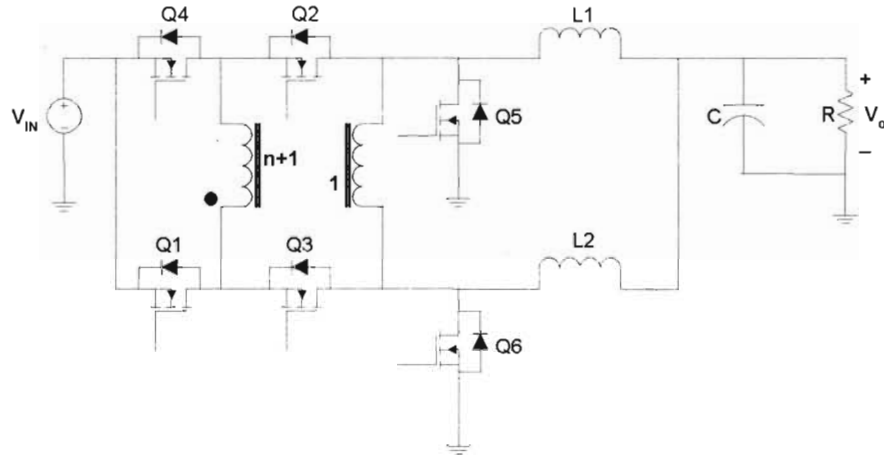


Figure 2.11 Multiphase Phase-Shift Buck VRM

It is clear that the extreme duty cycle is the fundamental of the current VRM solution. Extending the duty cycle is expected to be beneficial. To modify the duty cycle, the transformer concept is employed. A transformer introduces the turns ratio  $n$ , an additional design variable allowing one to get a more desirable duty cycle. Among converters using the transformer concept, the Phase-Shift full Bridge converter can also achieve soft switching, which helps further in the reduction of the switching loss. Since isolation is not needed in the 12 V VRM applications, phase-shift buck (PSB) converter is derived from the full bridge converter. The PSB converter uses an autotransformer.

With phase-shifted control of the primary switches, zero voltage-switching turn-off of  $Q_1$ - $Q_4$  can be achieved. In the power transfer mode of the phase-shift buck converter,  $Q_4$  and  $Q_3$  are both on. In this mode  $Q_6$  is off and  $Q_5$  is on for freewheeling. The one turn winding in the PSB converter also serves as part of the current doubler. The autotransformer directly transfers some energy in addition to pure transformer coupling which is a more efficient way. In freewheeling mode,  $Q_2$  and  $Q_3$  are on.  $Q_6$  and  $Q_5$  are also on in this mode. There is a dual mode when  $Q_1$  and  $Q_4$  are both ON. The DC voltage gain of the phase-shift buck converter is

$$M = \frac{V_O}{V_{IN}} = \frac{D}{n+1} \quad \text{Equation 2.25}$$

By choosing the turns ratio, the duty cycle can be modified to achieve the higher efficiency. For example, with 12 V input, 1 V output, and  $n=2$ , the duty cycle will be 0.25. Again, the duty cycle is much higher compared to the conventional buck. Experimental results for 12 V input, 1.3V/35 A output, 1 MHz phase shift converter has about 10% increase in efficiency compared to the multiphase buck [12]. It is worth mentioning that while the multiphase phase-shift buck provides higher efficiency, it requires more devices in terms of switches and autotransformer to achieve this. These additional devices will translate into more cost and more importantly, more real estate of the pc board.

#### 2.4.4 Multiphase Winding-Coupled Buck VRM

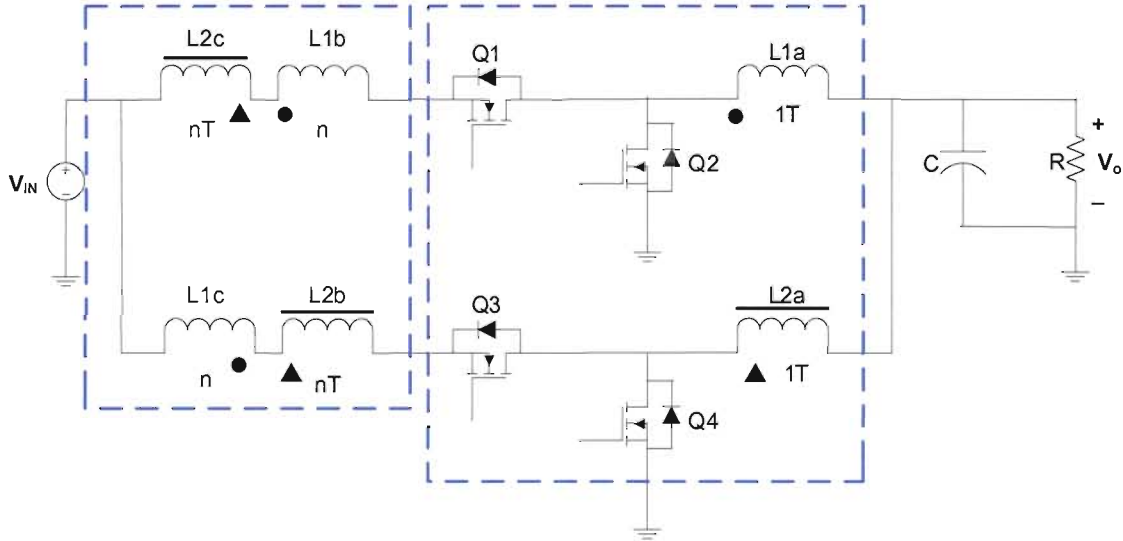
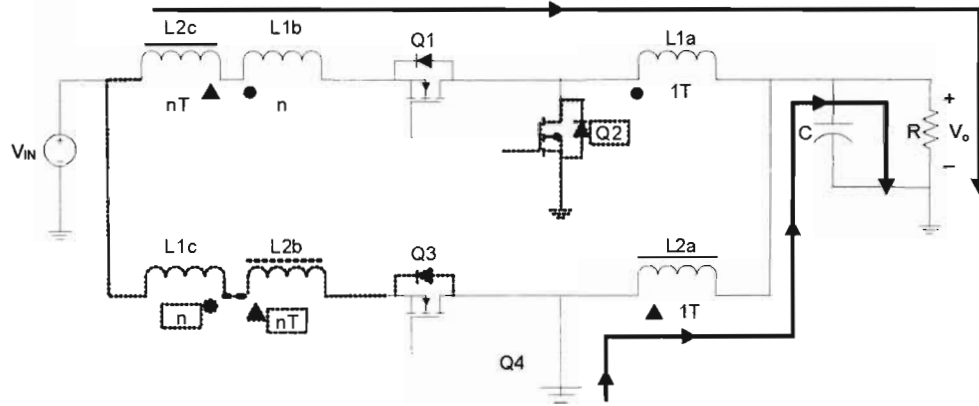


Figure 2.12 Multiphase Winding-Coupled Buck VRM

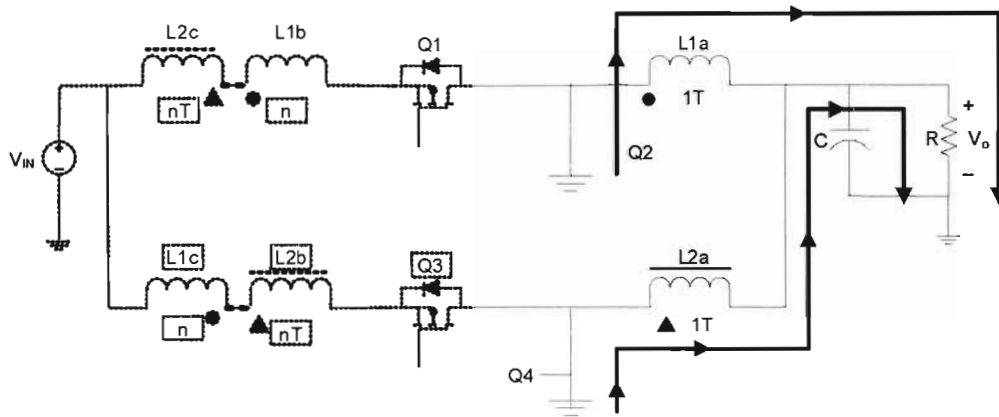
This novel topology significantly improves the efficiency without compromising the transient response. Figure 2.12 shows the Winding Coupled Buck Converter. In the right block it is a conventional buck converter with two phase interleaving. The two additional couple windings for each phase are shown in the left block. The first winding is coupled to the inductor in its phase and the second winding is coupled to the inductor in another phase. Both coupled windings have turns ratio of  $n$ . The control principle for the proposed converter is the same as that for a two phase interleaved buck converter. In the same phase the top and the bottom switches are controlled complementarily. For the different phases, they are controlled with  $180^\circ$  phase shifts. There are two operation stages. In stage I, one phase operates in the inductor charging period and the other phase operate in the freewheeling period. In stage II, both phases operate in the freewheeling period. In stage I,  $Q_1$  and  $Q_4$  are on and  $Q_2$  and  $Q_3$  are off.  $L_2$  operates as a transformer and  $L_1$  operates as an inductor. In stage II, both  $L_1$  and  $L_2$  operate as inductors to

freewheel the current to the output. The energy stored in winding  $L_{1b}$  in stage I is reflected to winding  $L_{1a}$  as in a flyback transformer. The DC voltage gain is the same as the phase-shift buck given as;

$$M = \frac{V_o}{V_{IN}} = \frac{D}{n+1} \quad \text{Equation 2.26}$$



(a)



(b)

Figure 2.13 (a) Stage I (b) Stage II

Figure 2.13 shows both stages of the converter. Again  $n$  is the turns ratio of the coupled inductors. For 12 V input, 1.5V/25 A at 1 MHz, the efficiency improvement is about 4% compared to the conventional buck converter [13]. One major drawback for

this topology is the voltage spike across the drain source of the top MOSFET due to leakage inductance. Lossless clamp circuit is needed to prevent the top MOSFET from being damaged or destroyed.

#### 2.4.5 Two-Stage Solutions VRM

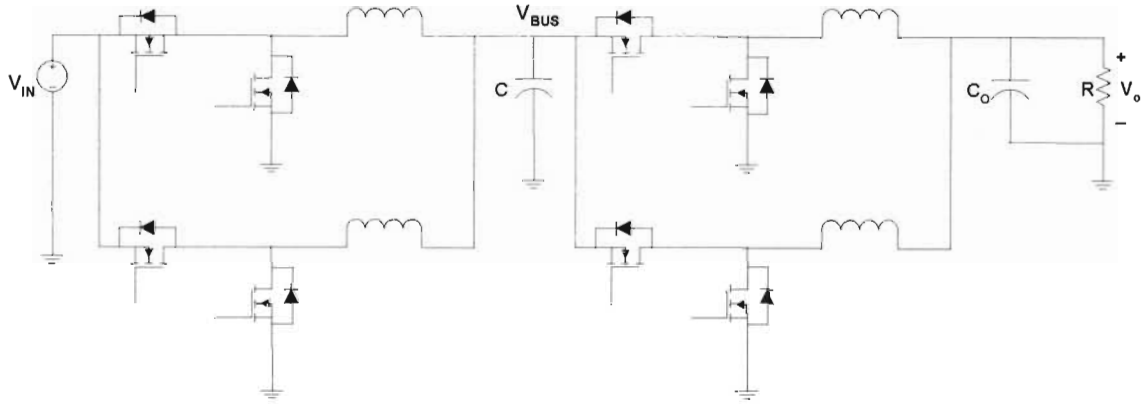


Figure 2.14 Two-Stage Solutions VRM

In order to deal with the stringent requirement of the future microprocessor, more and more capacitors have to be paralleled if low frequency approach is still followed. Compared with today's output capacitance, the bulk capacitance will increase by 2.5 times and the decoupling capacitance will increase 13 times in future. This is only possible by pushing the frequency of the VRM accordingly. Single stage multiphase VRM lacks the high frequency capability. The loss analysis illustrates that the major barriers are the switching loss and the body diode reverse recovery loss. It is well known that they are related with the input voltage. The lower the input voltage, the smaller the losses are. The concept of two stages VRM is proposed. The first stage which could be a simple buck converter, is used to step down the 12 V input to a certain intermediate bus voltage. The switching frequency of this stage is not necessarily high. Therefore

efficiency is very high. Experiments have shown that its efficiency at full load can reach 97%.

The second stage is still a multiphase buck converter. Compared with conventional single stage multiphase VRM, the only difference is the input voltage. Since the input voltage is much lower than 12 V, the switching loss and body diode reverse recovery loss can be significantly reduced. Besides that, low voltage rating device can be used instead of 30 V device to further improve the performance, Therefore the switching frequency can be pushed up to multi MHz while maintaining good efficiency. The overall voltage gain can be calculated as

$$M = \frac{V_O}{V_{IN}} = D_1 D_2 \quad \text{Equation 2.27}$$

where D1 and D2 are the duty cycles of the first and second stages, respectively.

According to experimental results as reported in for 12 V input, 1.2V/100A operating at 2 MHz, the overall system efficiency improvement is about 5% over the conventional buck operating at 500 kHz [14]. The two-stage approach promises to be more cost effective by reducing the number of output capacitors. It should be noted that the two-stage approach does not solve the technical challenges that the conventional buck faces.

## 2.5 Multiphase is the Way

As discussed in the previous sections numerous solutions have been proposed to resolve the technical conflicts of multiphase buck converters, such as extending duty cycle, improvement in transient performance, optimized current ripple in each channel and raising the switching frequency. However, the general problem remains the same: how to extend Moore's Law without introducing harmful functions, such as the thermal

cost, excessive components and electromagnetic interface problems. Figure 2.15 illustrates cost estimation of future voltage regulator modules. Today's 12 V input VRM widely used in industry is based on multiphase buck converters with interleaving technique. This technique not only experimentally proven can reduce current ripple to the output filter capacitors and improve the transient response, but also increase the power density. However, multiphase buck converters with interleaving technique only produces current ripple cancellation effect. In 2010, if the switching frequency for multiphase interleaving buck converters in range 300 kHz to 500 kHz is implemented, the voltage regulator module is estimated to occupy about 30% of a PC motherboard area due to the power requirements of future microprocessors [15]. If this power challenge is not resolved, the familiar trend of smaller, faster, low cost processors and devices could be compromised. Futuristic applications such as real time speech and facial recognition might never be realized further. It is predicted that improving the power supply efficiency of the 205 million PC's in the U.S. could reduce nationwide energy use by 1 to 2% and remove \$1 billion or more yearly electricity bills, while cutting emissions from generating plants.



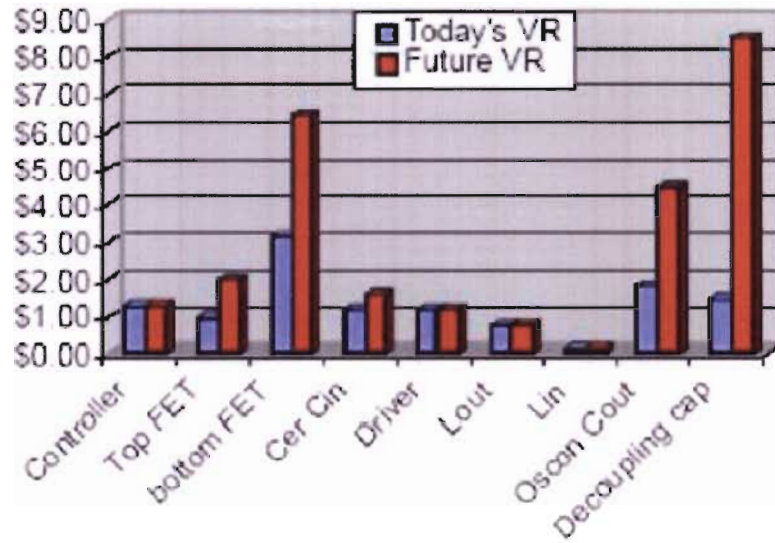


Figure 2.15 Cost Estimation of Future Voltage Regulator Modules

Therefore, to resolve the power challenge, three technical conflicts of multiphase interleaving buck converters are formulated as follows:

- If the output voltage is decreased, then the power consumption can be reduced but the duty cycle is also decreased, which result in poorer ripple cancellation effect and higher turn off losses on the top switches.
- If the switching frequency is increased, then the power density can be increased but the switching gate drive and body diode losses are also increased, which result in lower efficiency.
- If the inductance value is decreased, then the transient response can be improved but the current ripple in each cell also increased, which result in higher switching, conducting and winding losses.

Based on these technical conflicts analysis, it is clear that new converter architecture for future microprocessor is required. In recent years new converter topologies have been proposed to solve the technical conflicts discussed in previous sections. Extending the duty cycles is not enough due to the complexity of technical

conflicts that cannot be solved in one or two steps. The proposed two stage solution is an impractical approach since it is not really removing the technical conflicts

Multiphase buck converters with multi-interleaving technique perform better than with interleaving technique because multi-interleaving technique not only improves current ripple cancellation effect, but also generates switching frequency multiplication effect. Furthermore, the multi-interleaving technique can also extend duty cycle, improve transient response without increasing current ripple in each cell, and raise the switching frequency with low switching, gate drive and body diode losses [15]. This is the major reason behind the proposed new topology as explained in the following chapter.

## Chapter 3 Proposed Topology and Design Calculations

### 3.1 Proposed Multiphase Multi-Interleaving Buck Converter

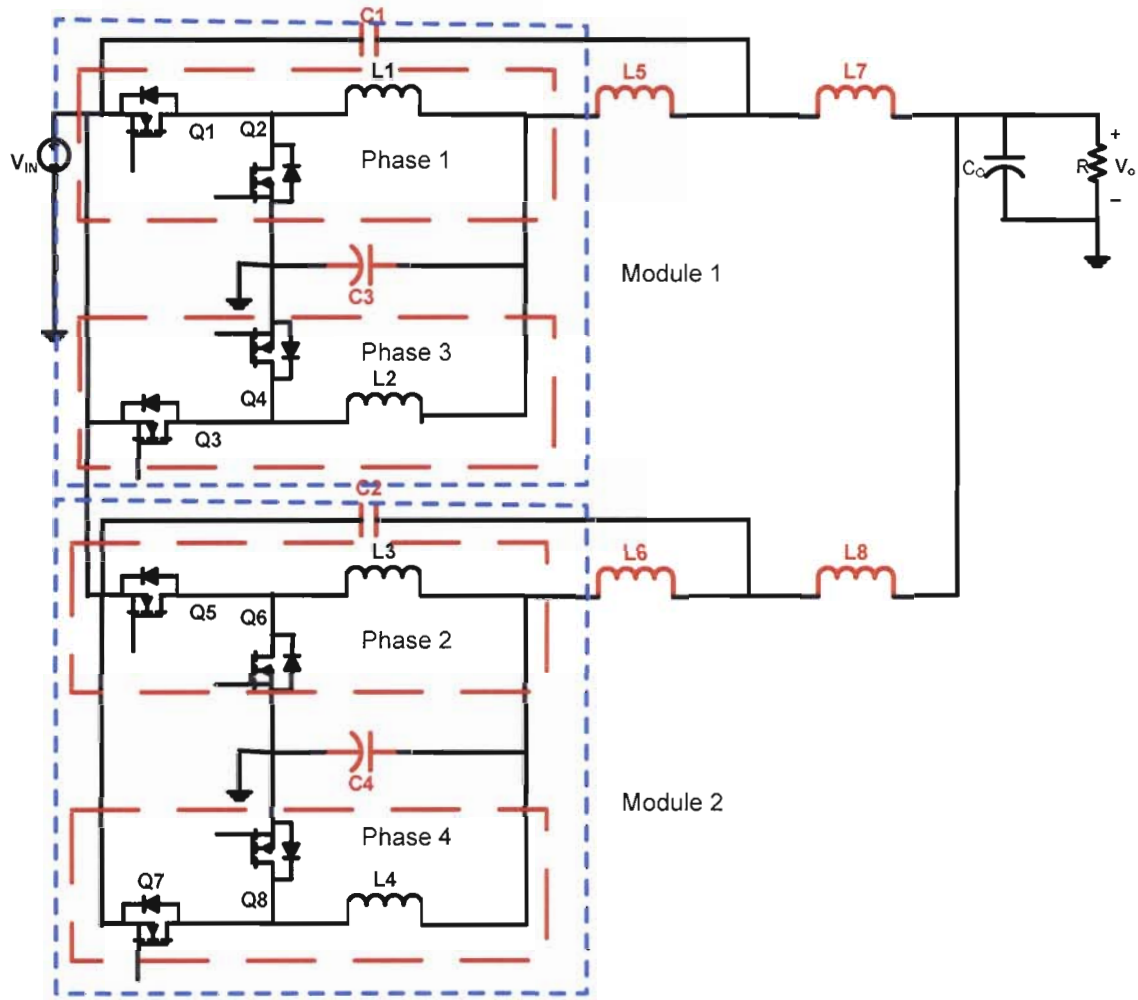


Figure 3.1 Proposed Multiphase Multi-Interleaving Buck Converter

To address several issues with present multiphase topologies as discussed in the previous chapter, a new topology is proposed. Figure 3.1 shows the proposed new multiphase multi-interleaving buck converter circuit. This multiphase circuit is composed of two modules and four phases or channels where each phase individually works as a synchronous buck converter. Within each module, there are two individual synchronous buck converters connected in parallel. Each module is then connected to other modules in

parallel as well to allow the interleaving operation. Here MOSFETs  $Q_1$ ,  $Q_3$ ,  $Q_5$  and  $Q_7$  are being used as the top switches, which have the conduction time of  $DT$ , the product of Duty Cycle  $D$  and switching period  $T$ . Whereas MOSFETs  $Q_2$ ,  $Q_4$ ,  $Q_6$  and  $Q_8$  are being used as the lower switches with conduction time of  $(1-D)T$ . Both inductor-capacitor pairs of  $L_5$ ,  $C_1$  and  $L_6$ ,  $C_2$  are the bypass components placed between input and output to increase the energy storage. Inductors  $L_7$  and  $L_8$  are the main output inductors for further filtering. Capacitor  $C_3$  is placed between the ground and the junction of individual output inductors  $L_1$ ,  $L_2$  of the first module and the bypass inductor  $L_5$ . Similarly capacitor  $C_4$  is placed between ground and the junction of individual output inductors  $L_3$ ,  $L_4$  of the second module and the bypass inductor  $L_6$ .

The proposed new topology is called multiphase multi-interleaving because not only that the switches turn on and turn off alternatively and sequentially between phases but also in between modules. In Figure 3.1, there are four phases in the proposed topology and by using  $360^\circ/N$ , where  $N$  is the number of phases in the circuit, each phase will be  $90^\circ$  apart from each other. However, in multiphase multi-interleaving the sequence of turning on of switches is slightly different than that of a simple multiphase buck. To illustrate this, refer to Figure 3.1, where there are two modules, each consisting of two phases. Let's start with MOSFET  $Q_1$  of module 1 and assume this is "phase 1". This switch is the first one to get turned on. After a delay of  $90^\circ$ ,  $Q_5$  which is the top switch of "phase 2" in module 2, has its turn to turn on. Then  $Q_3$  in "phase 3" of module 1 would turn on after a delay of  $180^\circ$  with reference to  $Q_1$ . Lastly  $Q_4$  in module 2 and "phase 4" turns on after  $270^\circ$  delay from  $Q_1$ . The timing signals of these top switches are shown in Figure 3.2.

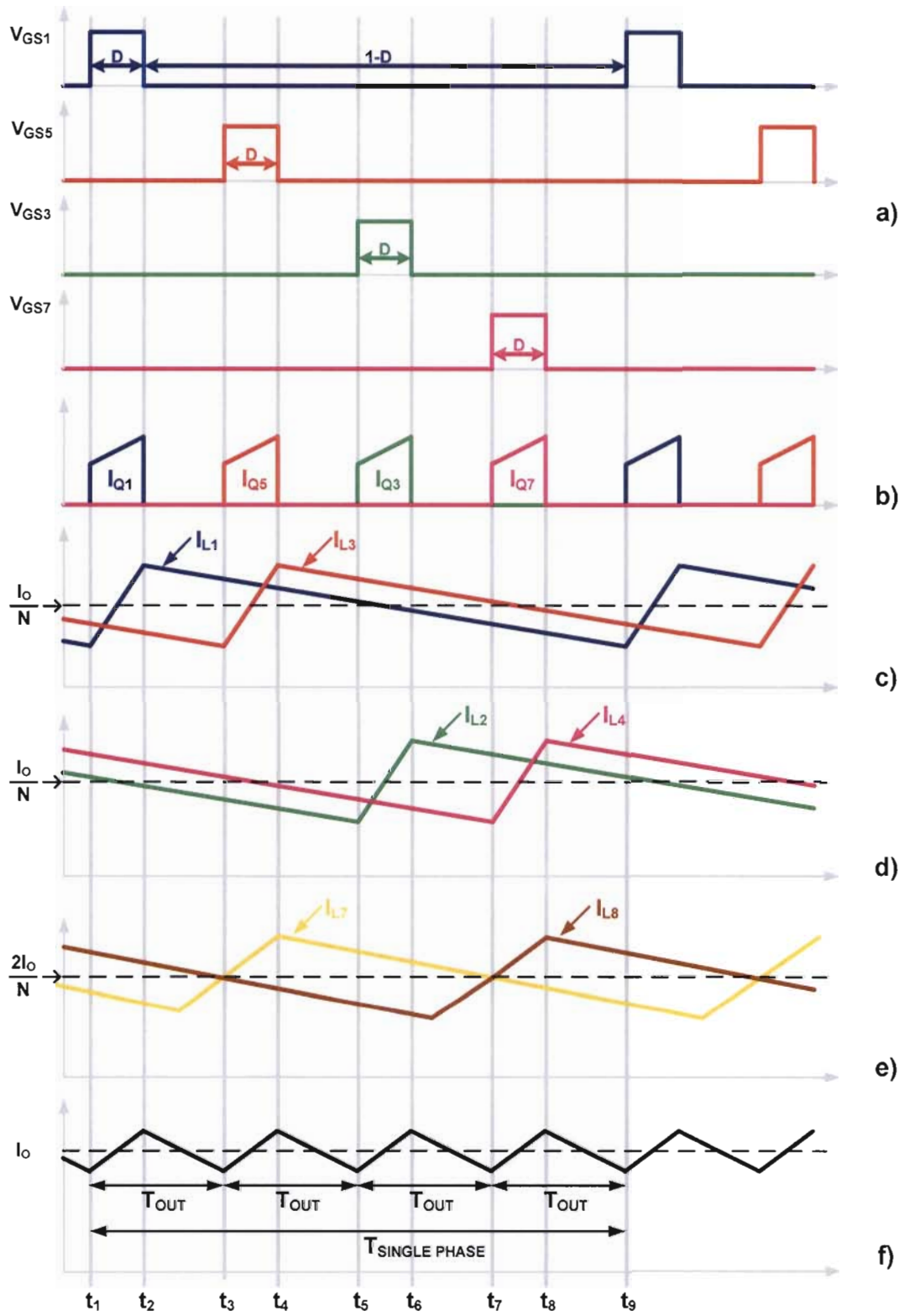


Figure 3.2 Key Waveforms of Proposed Multiphase Multi-Interleaving Buck Converter: (a) Upper FETs Gate Drive Signals, (b) Composite of Upper FETs current, (c) Inductor Current of  $L_2$  and  $L_4$ , (d) Inductor Current of  $L_3$  and  $L_4$ , (e) Output Current

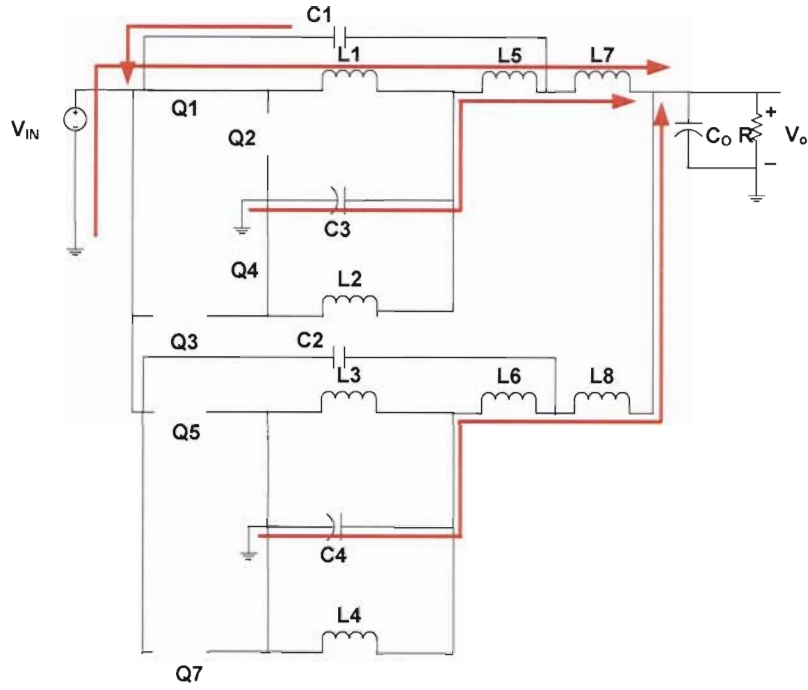


Figure 3.3 Equivalent Circuit of the Multiphase Multi-Interleaving Buck Converter From  $t_1$ - $t_2$

In steady state operation, when  $Q_1$  is turned on from  $t_1$ - $t_2$ , the current flows from the voltage source  $V_{IN}$  to the load  $R$  through  $Q_1$ ,  $L_1$ ,  $L_5$  and  $L_7$ . The current through  $Q_1$  increases linearly since it equals the inductor  $L_1$  current. By Ohm's law, the voltage across  $L_1$  is

$$V_{L1} = L_1 \frac{di_{L1}}{dt}$$

Consequently, the slope of its current is

$$\frac{di_{L1}}{dt} = \frac{V_{L1}}{L_1} \approx \frac{V_{IN}}{L_1} = \text{Constant}$$

This implies the inductor current charges up linearly. At the same time the energy stored previously in  $C_1$  is discharged to  $L_1$  via  $Q_1$ . Also  $C_3$  transfers its energy to  $L_5$  in that time since there is no other path for its energy to discharge.

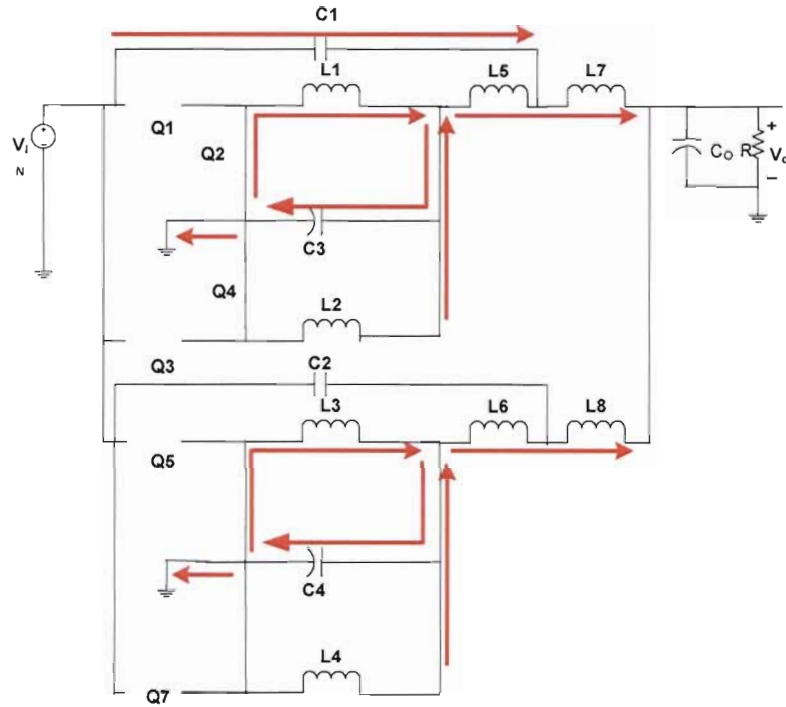


Figure 3.4 Equivalent Circuit of the Multiphase Multi-Interleaving Buck Converter From  $t_2$ - $t_3$

Figure 3.4 corresponds to  $t_2$ - $t_3$  when  $Q_1$  turns off and  $Q_2$  turns on.  $L_1$  was charged up when  $Q_1$  was on, and now it will be discharged through  $Q_2$ ,  $L_5$  and  $L_7$  to the load. In the mean time current will also flow from  $C_3$  to the ground and result in charging it up. During this the current flows directly from voltage source to the load through  $C_1$ - $L_7$  as well as through  $C_2$ -  $L_8$  and  $L_3$ - $L_6$ - $L_8$ .

The previous processes from  $t_1$ - $t_2$  and  $t_2$ - $t_3$  take place for every phase in each module. The output currents of two phases within a module add together which produces current ripple cancelation effect. This is further improved by pushing the current through the bypass and auxiliary inductors which further reduce the current ripple. In the end currents from both modules sum up before the capacitor  $C_0$  resulting in a final ripple cancellation. Another advantage this topology offers is the frequency multiplication

effect. Output current ripple frequency is greater than the input ripple current frequency by the number of phases employed in the proposed multiphase multi-interleaving buck converter. That means in the present example, the output frequency is 4 times that of the input frequency. The frequency multiplication helps in making the converter's physical size smaller because it decreases the output ripple current. The AC component of the output current decreases, which allows to use smaller capacitor in the output filter of the converter and helps in increasing the power density by decreasing the converter size. This benefit comes with the fact that the power loss at the input switches is not affected by the frequency multiplication and the loss in each switch remains proportional to single phase frequency.

### 3.2 Design Equations

The multiphase multi-interleave buck converter basically has the same design equations as that of a simple single-phase synchronous buck converter. In the design of multiphase multi-interleave buck converter, output voltage and output current are denoted by  $V_O$  and  $I_O$  respectively. There are  $N$  channels in multiphase multi-interleave buck converter where  $N$  represents the number of phases in the converter. Each channel can be regarded as an individual synchronous buck converter. The relation of output frequency and output current of multiphase multi-interleave converter with one phase of multiphase multi-interleave buck converter is

$$f_o = Nf_s \quad \text{Equation 3.1}$$

where  $f_o$  is the output frequency and  $f_s$  is frequency of single phase

$$I_o = NI_s \quad \text{Equation 3.2}$$

where  $I_o$  is the average output current



$I_s$  is the average output current of each phase

There are three major components in the multiphase multi-interleave buck converter to design:

- 1) Output Inductor for Each Phase
- 2) Main Output Capacitor
- 3) Input Capacitor at the Junction of Input and Ground

Output inductor design equation can be developed from the volt second balance at off time

$$V_L = L_O \frac{di}{dt} \quad \text{Equation 3.3}$$

Solving for  $L_O$ :

$$L_O = V_L \frac{dt}{di} \quad \text{Equation 3.4}$$

where  $di = \Delta I_{LCH}$  the ripple current through the output inductor of each channel,

Using  $dt = (1-D)T_s$  where  $T_s$  is the switching period, and  $D$  is the duty cycle,

Equation 3.4 becomes

$$L_O = \frac{V_O(1-D)T_s}{\Delta I_{LCH}} \quad \text{Equation 3.5}$$

or,

$$\Rightarrow L_O = \frac{V_O(1-D)}{\Delta I_{LCH} f_s} \quad \text{Equation 3.6}$$

Ideally,  $V_o$  is the average output voltage but in real design it is the output voltage plus drop across passive elements as shown in Equation 2.4.

The next component to design is the main output capacitor. The function of the capacitor is to hold the output voltage constant. In a real model of a capacitor, along with capacitance  $C$  there are two other associated quantities, namely the equivalent series resistance (ESR) and inductance (ESL). But at high frequency ESR is more dominant than ESL and so ESL can be neglected. The minimum capacitance can be calculated for multiphase converter by

$$C_o = \frac{\Delta I_L}{8f_s \Delta V_o} \quad \text{Equation 3.7}$$

The combined inductor current ripple to be filtered by the main output capacitor  $C$  can be found by using the graph of Figure 3.5 [16].

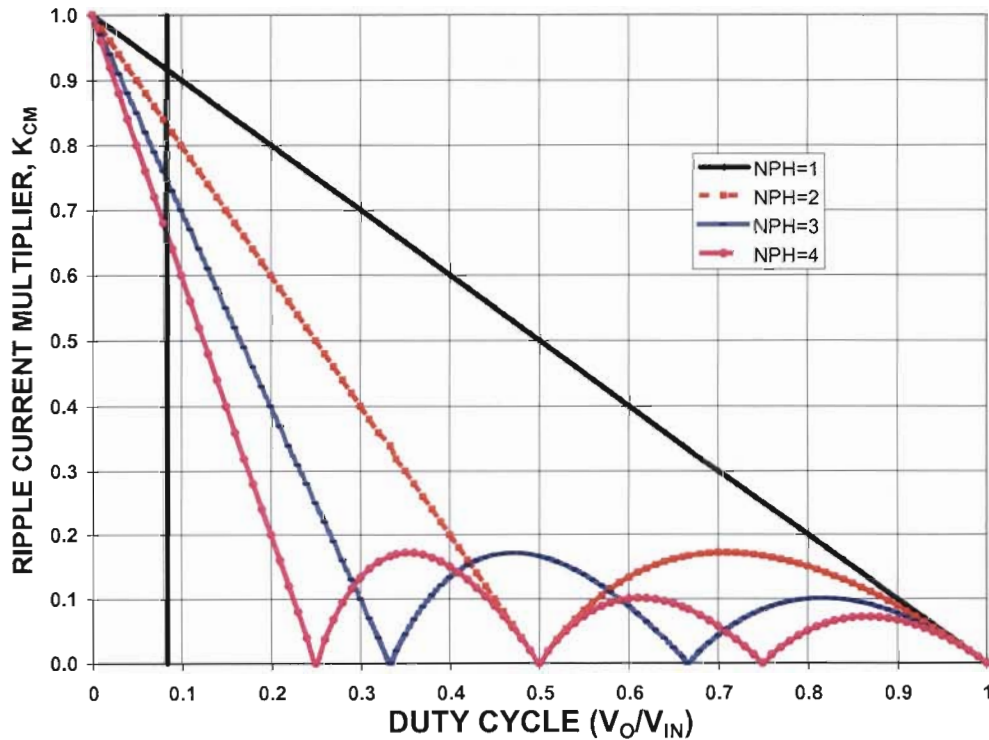


Figure 3.5 Output Ripple Current Multiplier for Various Phases

$$\Delta I_L = \frac{V_o(1-D)}{L_o f_s} \cdot \frac{N \left( D - \frac{m}{N} \right) \left( \frac{m+1}{N} - D \right)}{D(1-D)} \Rightarrow \Delta I_L = \frac{V_o}{L_o f_s} \cdot \frac{(N.D - m + 1)(m - N.D)}{N.D}$$

$$I_{RIPPLE} = \Delta I_L = K_{NORM} K_{CM} \quad \text{Equation 3.8}$$

$$\text{where } K_{NORM} = \frac{V_o}{L_o f_s} \text{ and } K_{CM} = \frac{(N.D - m + 1)(m - N.D)}{N.D}.$$

$m = \text{floor}(N.D)$  is the maximum integer that does not exceed the  $N.D$  [16],  $N$  is the number of phases and  $D$  is the duty cycle.  $K_{CM}$  is the ripple current multiplier.

Equation 3.8 can be re-written as:

$$\Delta I_L = \frac{V_o K_{CM}}{L_o f_s} \quad \text{Equation 3.9}$$

Generaily, ESR influences the capacitance value and it is given by

$$ESR \leq \frac{\Delta V_o}{\Delta I_L} \quad \text{Equation 3.10}$$

The third important component is the input capacitor. For calculating the input capacitor the input ripple current can be calculated by using the graph of Figure 3.6 [16].

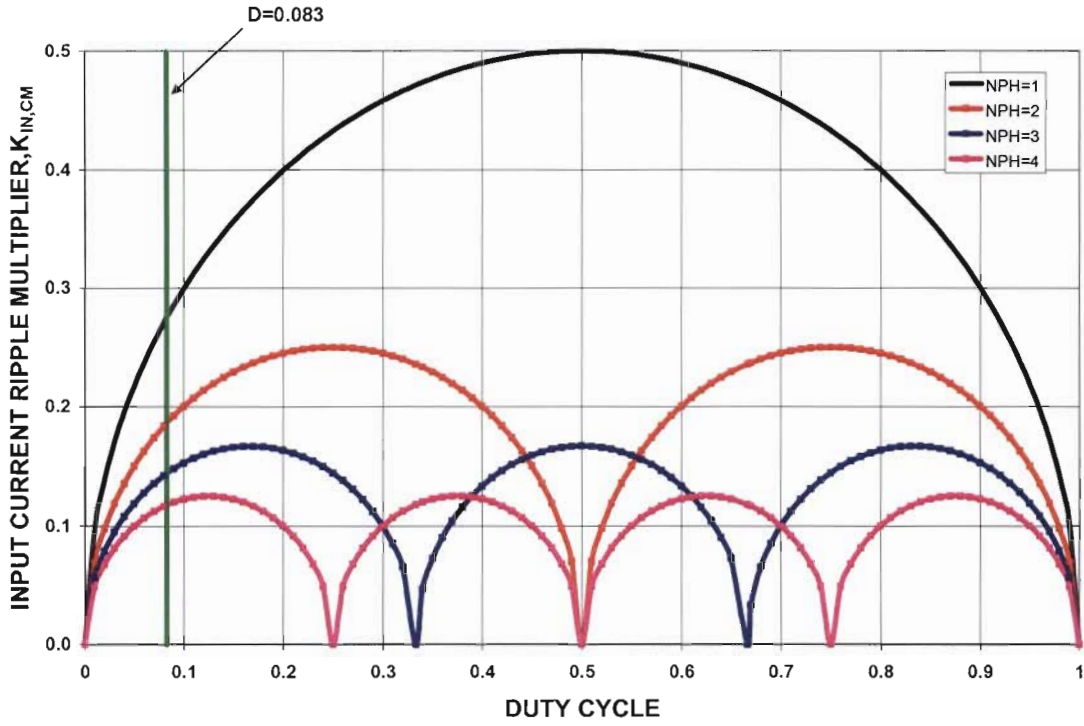


Figure 3.6 Input Ripple Current Multiplier for Various Phases

$$I_{INRipple} = I_{L,CH} K_{IN,CM} \quad \text{Equation 3.11}$$

The minimum input capacitance can be calculated from equation

$$i_c = C \frac{dV_{IN}}{dt} \quad \text{Equation 3.12}$$

Equation 3.11 can be written as

$$C = i_c \frac{dt}{dV_{IN}} \quad \text{Equation 3.13}$$

where  $i_c$  is equal to  $I_{INRipple}$ , therefore

$$C_{IN} = \frac{I_{INRipple} DT_S}{\Delta V_{IN}} \Rightarrow \frac{I_{L,CH} K_{IN,CM} DT_S}{\Delta V_{IN}} \quad \text{Equation 3.14}$$

even when the input voltage fluctuates. The efficiency of the converter should be greater than 80% at the maximum output current and nominal input voltage.

From electrical specifications now we can calculate the different components of the converter according to our needs which include capacitors, inductors, power MOSFETs, drivers and controllers.

### 3.3.1 Number of Phases

The four phases has been selected for the proposed multiphase multi-interleaving since it is the minimum number required for its operation. As mentioned earlier for multi-interleaving it is necessary to have two modules, and each module should have at least two phases. Also, since the switching frequency is 500 kHz, then the 4 phases will yield the output frequency of 2 MHz due to the frequency multiplication effect. In term of cost effectiveness, four phases has been found to be the optimum solution [18].

### 3.3.2 Duty Cycle

Duty cycle for the overall converter can be approximately calculated as:

$$D \approx \frac{V_o}{V_{IN}} = \frac{1}{12} = 0.0833$$

### 3.3.3 Controller selection

The proposed multiphase multi-interleaving DC-DC converter utilizes the Texas Instrument's TPS40090 multiphase controller and TPS2832 adaptive driver to step down a 12 V input to 1 V at 500 kHz [19],[20]. The TPS40090 provides fixed frequency, peak current mode control with forced current balancing. Phase currents are sensed by the voltage drop across the DC resistance of inductors. Other features include a single

voltage operation, true differential output voltage sense, user programmable current limit, capacitor programmable soft start and a power good indicator [16].

### 3.3.4 Switching Frequency

The clock oscillator frequency for the TPS40090 is programmed with a single resistor from  $R_T$  (pin 16) to signal ground. Equation from the data sheet allows selection of the  $R_T$  resistor in  $k\Omega$  for a given switching frequency in kHz [16] as shown below:

$$R_T = K_{PH} \times (39.2 \times 10^3 \times f_{PH}^{-1.041} - 7) K\Omega \quad \text{Equation 3.15}$$

where

$K_{PH}$  is the coefficient that depends on the number of active phases

$f_{PH}$  is the single-phase frequency, in kHz

For 4-phase  $K_{PH} = 1.0$  is a single-phase frequency, in kHz

The  $R_T$  resistor value in last expression is given in  $k\Omega$ . For 500 kHz switching frequency,  $R_T$  is calculated to be 53.76  $k\Omega$ . However, due to unavailability, a resistor with 53.6  $k\Omega$  value is used instead.

### 3.3.5 MOSFET Selection

For the upper MOSFET, the dynamic or switching losses are the predominant factors, and conduction losses play a secondary role because the duty cycle is very small and less than 10%. The conduction time is very small as compared to the number of switching from one state to another in one second. The MOSFET should meet the voltage and current specification with as low a gate charge as possible to keep the dynamic losses small. Consequently, a MOSFET with a moderate  $R_{DS,ON}$  will be desirable. For that reason we chose FDS8690 [21]. It is an N channel power trench

MOSFET with rating of  $V_{DS} = 30$  V and drain current  $I_D = 14$  A. Its  $R_{DS,ON}$  is 11.4 m $\Omega$  with gate charge  $Q_G = 14$  nC.

For the synchronous rectifier switch or the lower MOSFET, it must meet the voltage and current requirements of the application. It must also have a sufficiently low  $R_{DS,ON}$ , so that the conduction loss should remain small enough to meet the efficiency target. The  $R_{DS,ON}$  is the on state resistance from drain to source. The conduction time of the lower switch is much larger than the upper switch due to small duty cycle. That is why it is required to have lower  $R_{DS,ON}$  for lower conduction losses. For this MOSFET, the gate charge plays a secondary role in power dissipation. For that reason we chose FDS6299S [22]. It is an N channel power trench MOSFET with rating of  $V_{DS} = 30$  V and drain current  $I_D = 21$  A. Its  $R_{DS,ON}$  on is 5.14 m $\Omega$  with gate charge  $Q_G = 43$  nC.

Calculations for MOSFET selection are shown in Table 3.2 and 3.3.

High Side MOSFET	$R_{DS(ON)}$ @ 4.5V [m $\Omega$ ]	$Q_G$ @ 5V [nC]	Switching Loss [W]	Conduction Loss @ 5V [W]	Sum of Conduction & Switching Losses @ 5 V [W]	Total Loss at 4 Switches [W]
Si7860DP	11.000	18	0.023	0.092	0.114	0.458
Si7386DP	10.000	18	0.023	0.079	0.102	0.408
Si7686DP	14.000	14	0.018	0.117	0.135	0.538
FDS8690	11.000	14	0.018	0.095	0.113	0.451
FDMS8674	8.000	20	0.025	0.067	0.092	0.368
FDS8817NZ	10.000	24	0.030	0.084	0.114	0.454
FDMS8680	11.000	26	0.033	0.092	0.124	0.498
FDD8780	12.000	16	0.020	0.100	0.120	0.481

Table 3.2 Calculations for High Side MOSFET Selection

Low Side MOSFET	$R_{DS(ON)} @ 4.5V [m\Omega]$	$Q_G @ 5V [nC]$	Switching Loss [W]	Conduction Loss @ 5V [W]	Sum of Conduction & Switching Losses @ 5 V [W]	Total Loss at 4 Switches [W]
Si7880ADP	4.000	55	0.069	0.368	0.437	1.747
Si7336ADP	4.000	50	0.063	0.368	0.430	1.722
Si7192DP	2.225	66	0.083	0.205	0.287	1.149
Si7658DP	3.250	75	0.094	0.299	0.393	1.571
SiE806DF	2.100	115	0.144	0.193	0.337	1.348
SUB85N03-04P	7.000	90	0.113	0.644	0.756	3.025
FDS6299S	5.100	43	0.054	0.469	0.523	2.091
FDS6699S	4.500	49	0.061	0.414	0.475	1.901
FDS8672S	7.000	21	0.026	0.644	0.670	2.680
Si4642DY	4.700	54	0.068	0.432	0.500	1.999
STD150NH02L	4.000		0.000	0.368	0.368	1.472

Table 3.3 Calculations for Low Side MOSFET Selection

### 3.3.6 Output inductor

By using Equation 3.6 and taking 10% ripple of the individual phase because  $I_{Ripple}$  is usually chosen to be between 10% and 40% of maximum phase current [16], the output inductor is calculated as:

$$L_o = \frac{V_o(1-D)}{\Delta I_{LCH} f_s} = \frac{1(1-0.083)}{(0.1 \times 10)500 \times 10^3} = 1.83 \times 10^{-6} H$$

Other important factors to be considered when selecting the inductor are its maximum DC or peak current and maximum operating frequency. Using the inductor within its DC current rating is important to ensure that the inductor does not overheat. Operating the inductor at less than its maximum frequency rating ensures that the maximum core loss is not exceeded, preventing it from overheating or saturation.

Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for DC-DC converters, some of which are surface mountable. There are many



types of inductors available; the most popular core materials are ferrites and powdered iron. We chose the MLC1260-172ML inductor from Coilcraft with 1.75uH and DCR of 2.84mΩ because of its low DCR and physical size [26].

### 3.3.7 Output ripple cancellation and output capacitor selection

Due to interleaving of channels, the total output ripple current is smaller than the ripple current from a single phase. The output ripple current is given by equation 3.9:

$$\Delta I_L = \frac{V_O K_{CM}}{L_O f_s} \quad [A]$$

From Figure 3.5 the value of  $K_{CM}$  is 0.67, and so:

$$\Delta I_L = \frac{V_O K_{CM}}{L_O f_s} = \frac{1 \times 0.67}{1.75 \times 10^{-6} \times 500 \times 10^3} = 0.765 A$$

The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple as given in equation 3.7:

$$C_O = \frac{\Delta I_L}{8 f_s \Delta V_O} = \frac{0.765}{8 \times 500 \times 10^3 \times 50 \times 10^{-3}} = 3.825 \times 10^{-6} F$$

In this design the  $C_{o(min)}$  is 3.825uF with  $V_{Ripple} = 50mV$ . However this affects only the capacitive component of the ripple voltage and the final value of the value of capacitance is generally influenced by ESR.

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.765} = 65 \times 10^{-3} \Omega$$

To limit the ripple voltage to 50 mV, the capacitor's ESR should be less than the value calculated of 65 mΩ. Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of

a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded.

An additional consideration in the selection of the output inductor and capacitor values can be derived from examining the transient voltage overshoot which can be initiated with a load step from full load to no load. By equating the inductive energy with the capacitive energy, the equation can be derived [16]:

$$C_{OUT} = L \frac{I^2}{V^2} = L_{EQ} \frac{((I_{OH})^2 - (I_{OL})^2)}{(V_{OUT2})^2 - (V_{OUT1})^2} = \frac{(1.83 \times 10^{-6})}{4} \frac{(40)^2}{((1.25)^2 - (1.0)^2)} = 1301 \times 10^{-6} F$$

Three capacitor technologies—low-impedance aluminum, organic semiconductor, and solid tantalum are suitable for low-cost commercial applications. Low-impedance aluminum electrolytic capacitors are the lowest cost and offer high capacitance in small packages, but ESR is higher than those of the other two types. Organic semiconductor electrolytic capacitors, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds—a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but much of the size and performance advantage is sacrificed. Solid-tantalum chip capacitors are probably the best choice if surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume [10].

The minimum output capacitance required to keep the output voltage ripple at 50mV is 3.825uF with ESR limitation of 65mΩ. To accommodate low ESR, the capacitors are placed in parallel so that the equivalent capacitance should be larger while the equivalent resistance get smaller. We have used six AVX TPSD227\*010#0050 capacitors in parallel [27]. Each capacitor has voltage rating of 10V with 50mΩ ESR.

### 3.3.8 Input Capacitor Selection

The bulk input capacitor selection is based on the input voltage ripple requirements. Due to the interleaving of multiphase, the input rms current is reduced. The input ripple current is calculated from Equation 3.11:

$$I_{IN,RMS} = I_{L,CH} K_{IN,CM} \quad [A]$$

$K_{IN,CM}$  can be found from graph in Figure 3.6 and is 0.12 for four phases, hence:

$$I_{IN,RMS} = I_{L,CH} K_{IN,CM} = 10 \times 0.12 = 1.2A$$

where  $I_{L,CH}$  is the inductor current in each phase.

The minimum input capacitance can then be calculated from Equation 3.14:

$$C_{IN} = \frac{I_{IN,RMS} DT_S}{\Delta V_{IN}} \Rightarrow \frac{I_{L,CH} K_{IN,CM} DT_S}{\Delta V_{IN}} = \frac{1.2 \times 0.083 \times 2 \times 10^{-6}}{100 \times 10^{-3}} = 2 \times 10^{-6} F$$

It is also important to consider a minimum capacitance value, which limits the voltage ripple to a specified value if all the current is supplied by the on-board capacitor. For a typical ripple voltage of 100mV the maximum ESR is calculated:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{100 \times 10^{-3}}{1.2} = 83.3 \times 10^{-3} \Omega$$

We are using Vishay OS-CON 94SVP107X0020E12 Aluminum Organic Capacitor which has a capacitance of 100μF and maximum ESR of 25mΩ with a rated voltage of 20V [23]. Two capacitors have been used in parallel to reduce the ESR value

and increase the capacitance. Nichion's UCD1E221MNL1GS Aluminum Electrolytic Capacitor with ratings of 25V and 220 $\mu$ F has been used in parallel with other two OS-CON capacitors to filter out the input current spikes.

Two different input supplies have been used in this circuit. A 12V supply is being used to power up the controller and 5V supply is being used for drivers. We have used the Nichion's OS-CON Aluminum Organic Capacitor PCJ1A121MCL1GS for the 5V supply as an input capacitor [25]. Its rated voltage is 10V and its ESR is 25m $\Omega$  with 120 $\mu$ F capacitance.

## **Chapter 4    Simulation of Proposed Topology**

### **4.1   Design Simulations**

Using the design calculations in section 3.3, the proposed multiphase multi-interleave buck converter is simulated in Cadence Capture CIS. Figure 4.1 represents the open loop schematic of the multiphase multi-interleave buck converter. The MOSFETs are modeled with IRF150 and the diode MBR340. The input power supply is modeled by a constant voltage source  $V_{in}$ . The gate signals to the MOSFETs are generated by using  $V_{pulse}$ . The schematic is simulated for the runtime of 2ms to ensure the simulation reaches steady state.

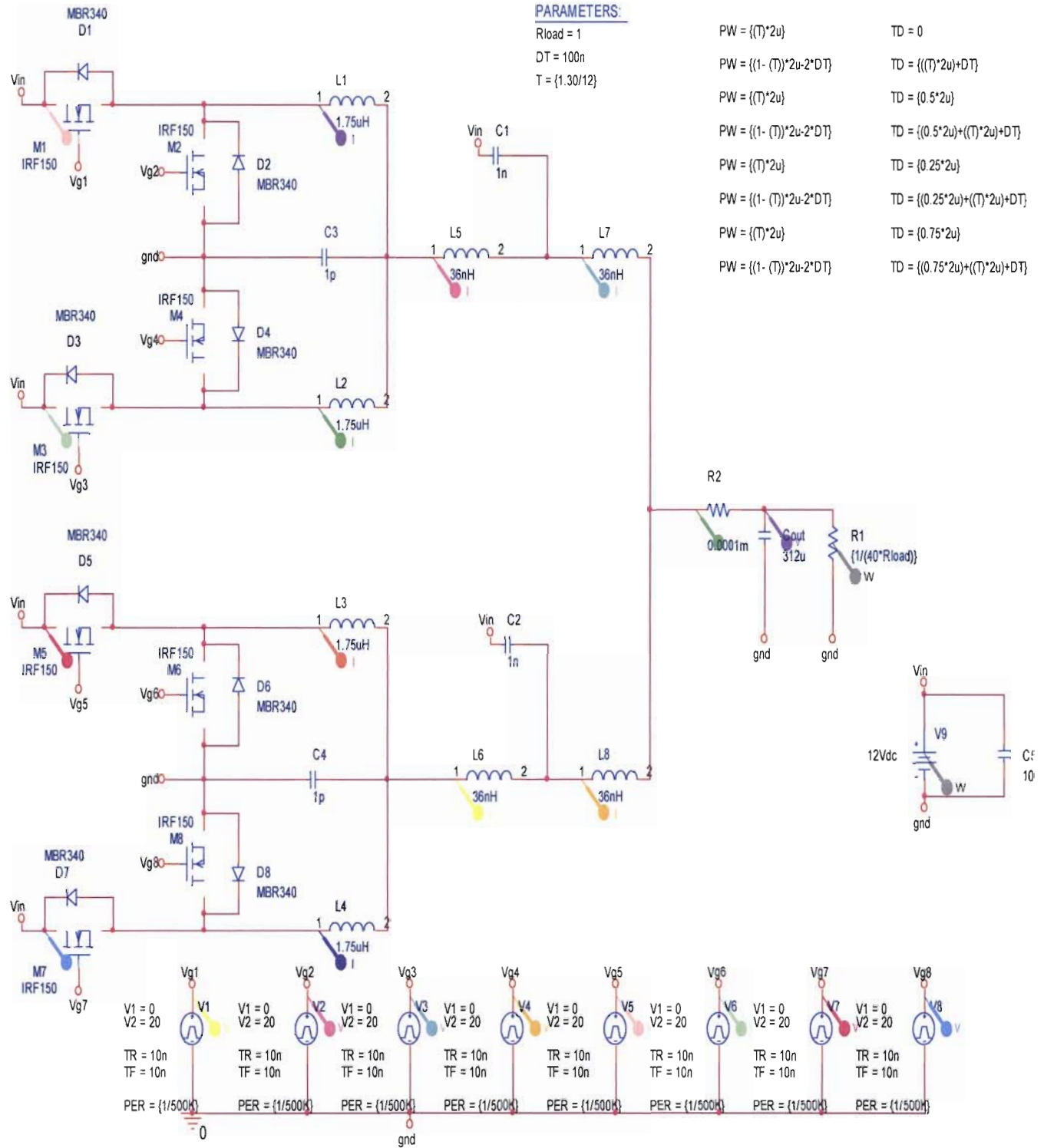


Figure 4.1 Open Loop Schematic of Proposed Multiphase Multi-interleave Buck Converter

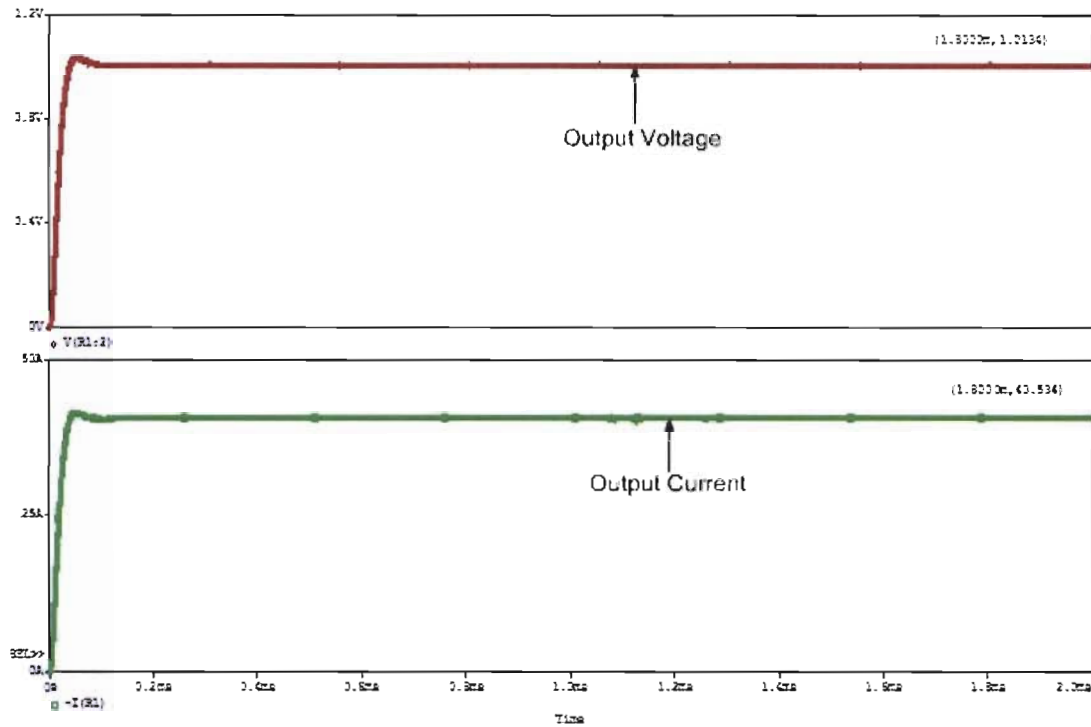


Figure 4.2 Instantaneous Output Voltage and Output Current at Full Load

The top graph in Figure 4.2 shows the output voltage of the circuit and the lower graph depicts the output current. The output voltage and output current reach the steady state at 0.1 ms with values 1.0134 V and 40.534 A at 1.8 ms respectively which meet our specification mentioned in Table 3.1. The average value of the output voltage is 1.0053 V which is nearly equal to the specification and represented in Figure 4.3. Figure 4.4 shows the close up of output voltage ripple where highest point of the ripple is at 1.0135 V and the lowest point is at 1.0134 V which makes the ripple very small at about 0.1 mV. The output switching frequency is calculated from Figure 4.4 by subtracting the time instances of two consecutive cycles which is 2  $\mu$ s, giving us exactly 2 MHz of output frequency.

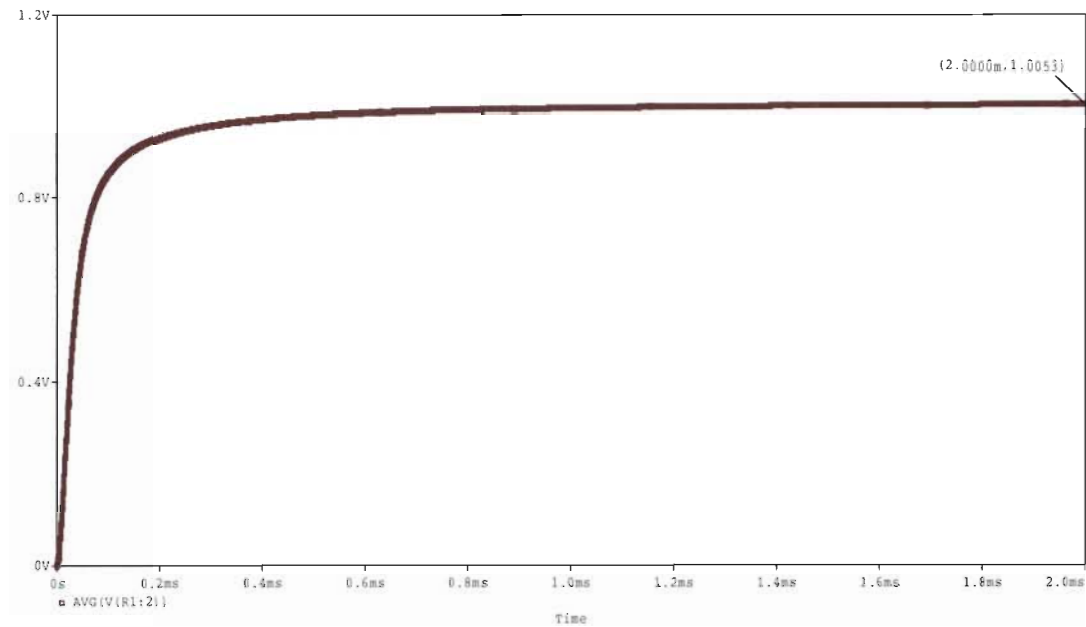


Figure 4.3 Average Output Voltage at Full Load

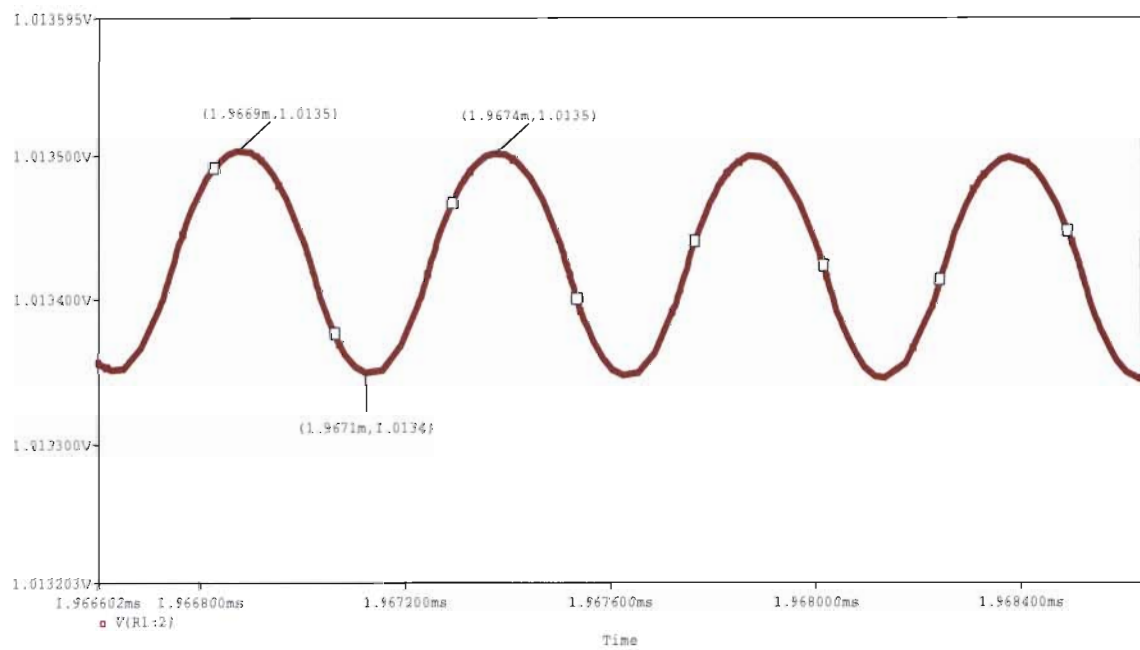


Figure 4.4 Output Voltage ripple at Full Load



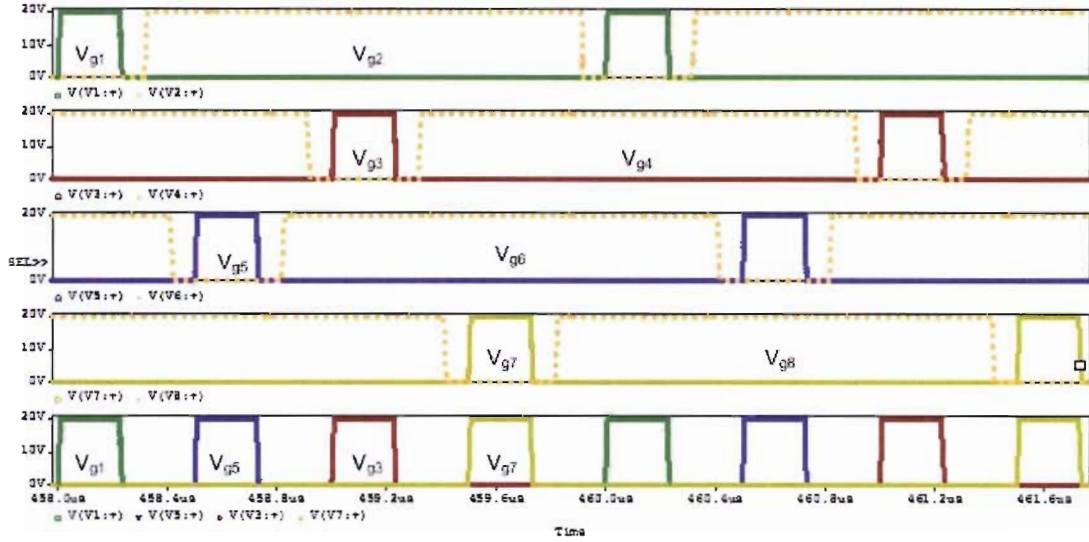


Figure 4.5 Simulation of Gate Signals for MOSFETs

As explained in Chapter 3, the parallel buck cells are switched at specific phase angles given by  $360^\circ/N$  where  $N$  is the number of phases. For four-phase buck, the phase angles are evenly distributed by  $90^\circ$  but as mentioned before, because of the multi-interleaving, phase 3 will turn on right after the turn off of phase 1. So the distribution angle remains  $90^\circ$  but the sequence of turning on is phase 1, phase 3, phase 2 and in the last phase 4. Two switching periods have been shown in Figure 4.5. The composite at the very bottom of this plot shows the overall output switching frequency, increases by  $N$  times each phase. In this case, it is 4 times the individual phase switching frequency.

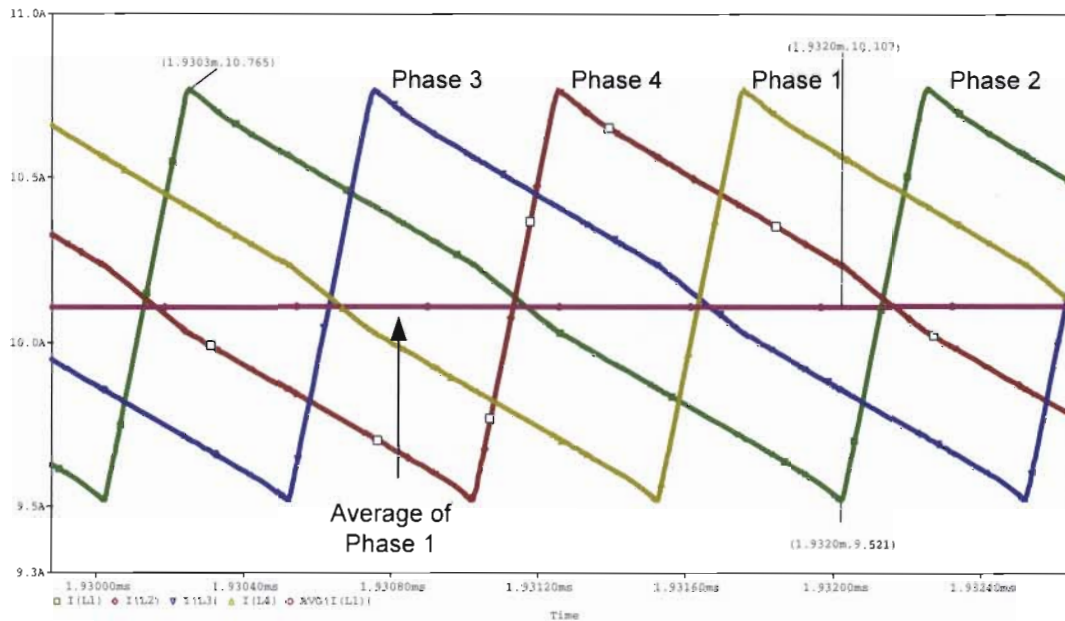


Figure 4.6 Output Inductor Current Waveforms at Each Cell at Full Load

The key advantage of multiphase multi-interleaving, which is current ripple cancellation, is cross checked by the simulation result in Figure 4.6. The ripple current cancellation effect can be observed since the inductor current for the different phases overlap one another. The ripple is calculated to be 1.244 A with maximum value at 10.765 A and minimum value of 9.521 A. The average value of inductor current is 10.107 A per phase.

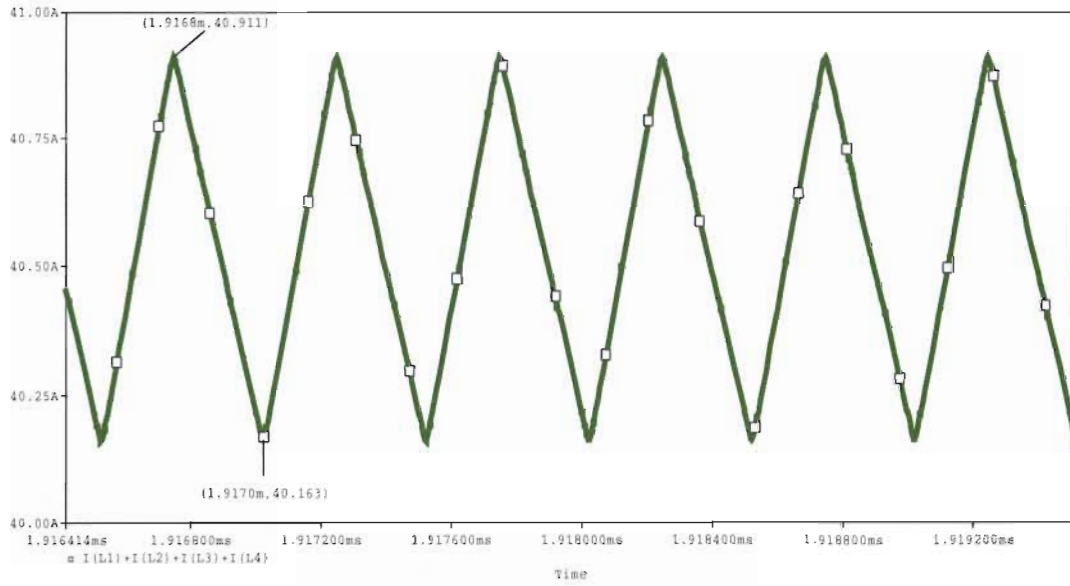


Figure 4.7 Sum of Output Inductor Currents for all Four Phases at Full Load

Output current ripple cancellation effect can be seen by summing up all four individual phase inductor currents. Figure 4.7 shows the summed inductor currents which has a maximum peak at 40.911 A and the minimum peak value at 40.163 A. After summing the output current, the ripple is found to be 0.75 A which is smaller than the individual phase inductor current ripple and proves the current ripple cancellation effect. The ratio of the summed output inductor current to the individual output inductor current is :

$$\frac{\text{Sum of Output Inductor Current Ripple}}{\text{Individual Output Inductor Current Ripple}} = \frac{0.75A}{1.244A} = 0.604 \quad \text{Equation 4.1}$$

From Figure 3.5,  $K_{CM}$  is 0.67 using duty cycle value of 0.083 and four phases. Our simulated value is close to the theoretical  $K_{CM}$  value of 0.67.

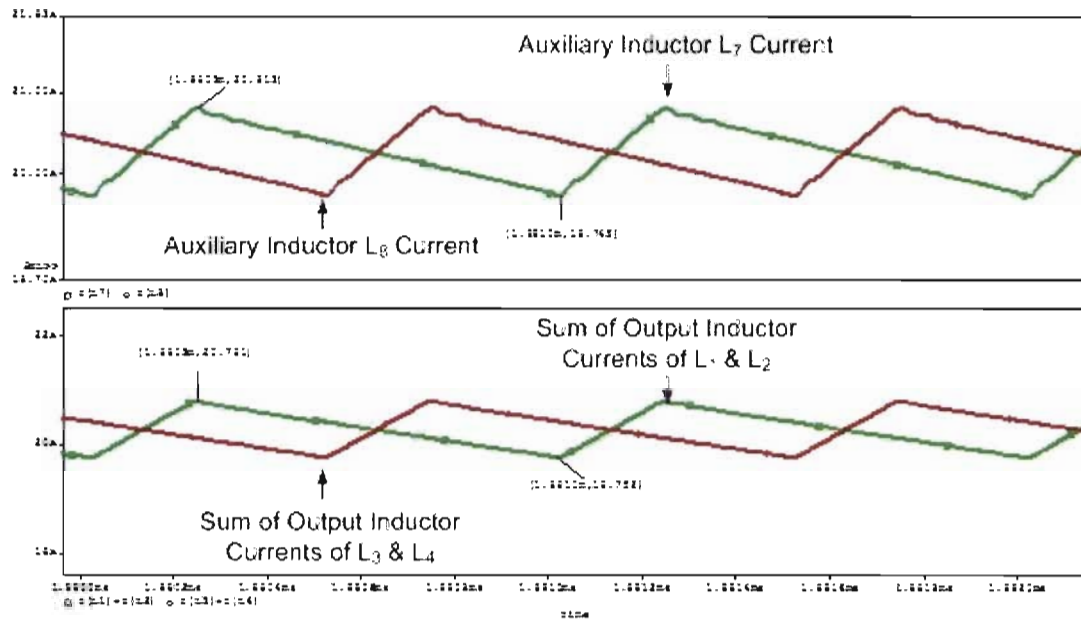


Figure 4.8 Auxiliary Inductor Current Waveforms at Full Load

Figure 4.8 top graph shows the individual auxiliary inductor currents with maximum current at 20.813 A and minimum current at 19.745 A. The bottom graph represents the combined currents of two phases of each module, showing a maximum peak at 20.791 A and a minimum peak at 19.752 A. If we look closely at Figure 4.1, it is clear that not all of the four inductor currents get combined right away. First the output inductor currents  $I_{L1}$  and  $I_{L2}$  of module 1 get combined and passed through the bypass and auxiliary inductor  $L_5$  and  $L_7$  respectively. In the same way output inductor current  $I_{L3}$  and  $I_{L4}$  of module 2 combine first and then pass through  $L_6$  and  $L_8$ .

After passing through auxiliary inductors, current of both modules add to each other. This shows that current ripple cancellation takes place in two steps, when the output inductor currents of two phases of the same module combine and when the output currents of two modules combine.

Figure 4.9 shows the sum of the auxiliary output inductor currents,  $I_{L7}$  and  $I_{L8}$ . The maximum peak value is 40.925 A and the minimum peak value is 40.150 A with a ripple of 0.775. Here the result which was obtained from Figure 4.7 can be verified.

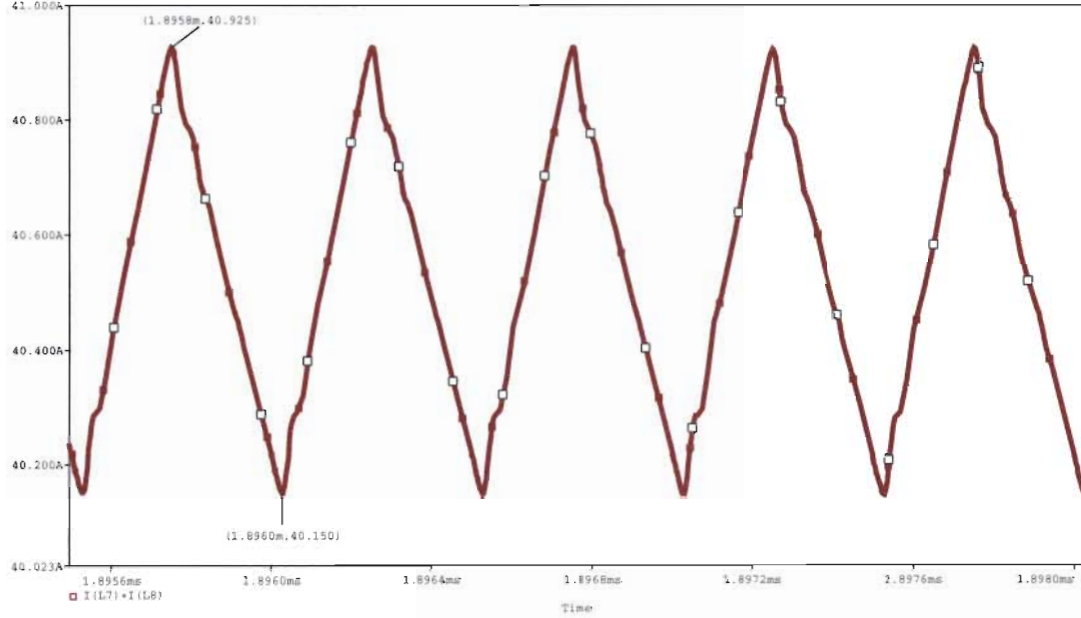


Figure 4.9 Sum of Auxiliary Inductor Currents Waveform at Full Load

The following ratio can now be calculated:

$$\frac{\text{Sum of Output Inductor Current Ripple}}{\text{Individual Output Inductor Current Ripple}} = \frac{0.775A}{1.244A} = 0.623$$

This is very close to the previous result of 0.604 and the theoretical  $K_{CM}$  factor 0.67. The above simulation result verifies the output ripple cancellation effect of the proposed multiphase multi-interleave buck. It also verifies the plot in Figure 3.5 which shows that at the smaller duty cycles, the ripple current multiplier  $K_{CM}$  gets smaller as the number of phase increases. Thus the ripple current can be significantly reduced with the increasing number of phases.

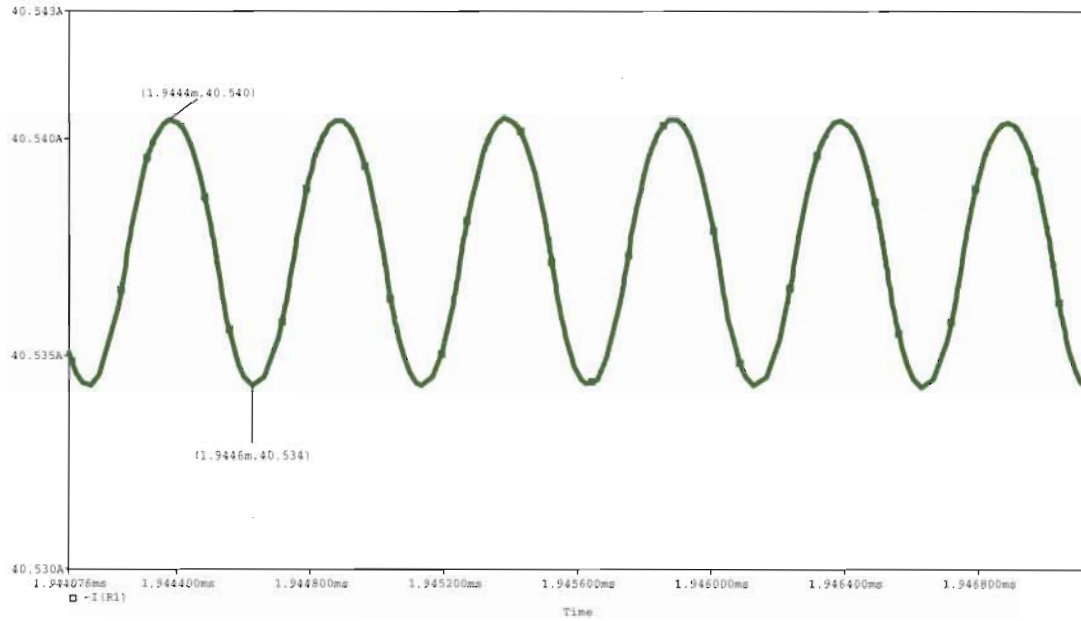


Figure 4.10 Output Current Waveform at Full Load

Figure 4.10 shows the output current waveform with the maximum peak of 40.540 A and the minimum value of 40.534 A with a small output current ripple of 6 mA. The small output ripple current is the result of the output capacitor which is filtering the inductor current. Figure 4.11 shows the simulated efficiency graph of multiphase multi-interleave buck, where at full load the efficiency is 69.485 %. The efficiency at the different load currents, from 10% load to full load has been plotted in Figure 4.12. The highest efficiency is 84.4 % at 8 A which is 20 % load. Table 4.1 shows the proposed converter's simulated efficiency.

$I_o$ [A]	Efficiency [%]
4	84.00
8	84.40
12	82.65
16	80.45
20	78.36
24	76.35
28	74.50
32	72.50
36	71.08
40	69.50

Table 4.1 Simulated Efficiency of the Proposed Converter at Different Output Currents

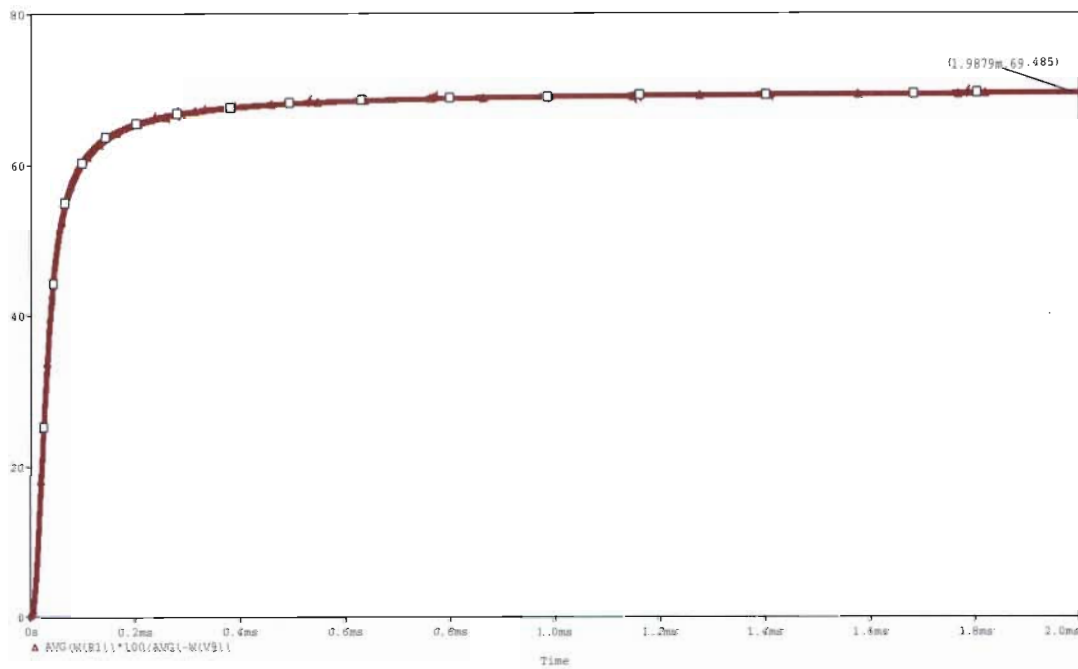


Figure 4.11 Efficiency Waveform at Full Load

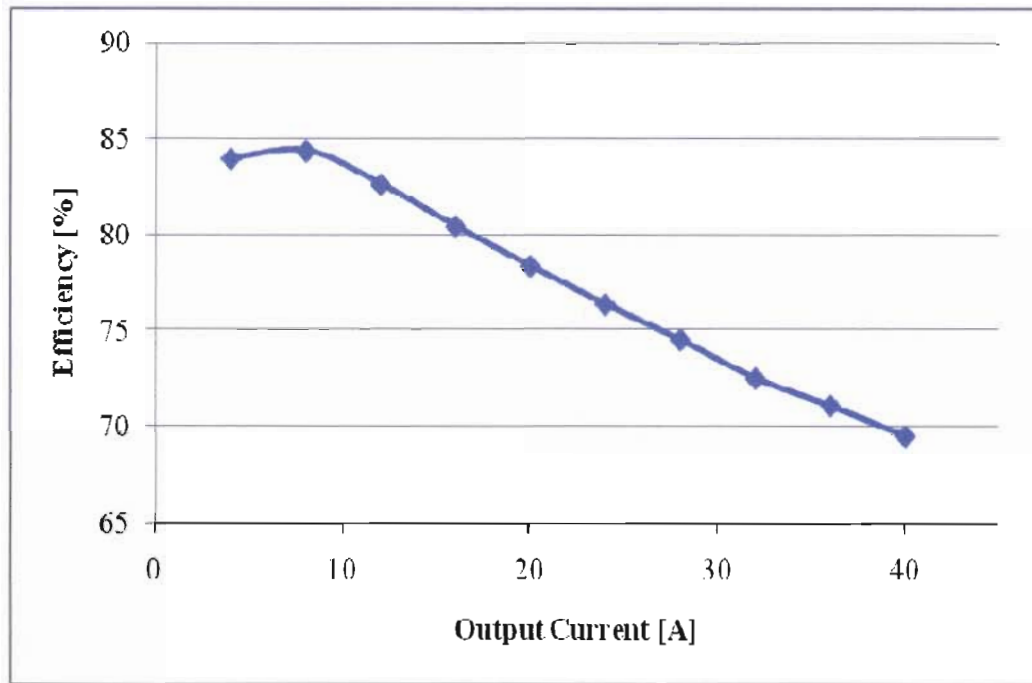


Figure 4.12 Efficiency vs. Load Current

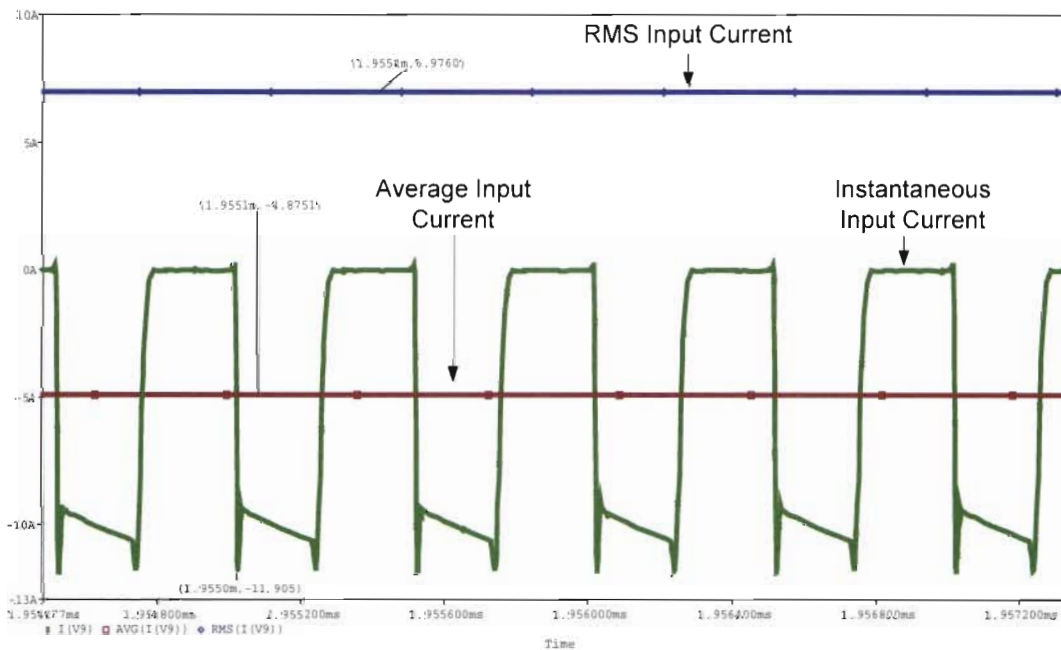


Figure 4.13 Input Current Waveform at Full Load

The upper MOSFET in synchronous buck topology draws the input current when it is turned on. In our simulation case, the input current has four peaks in every 2  $\mu$ s



because four MOSFETs are present in the circuit. The magnitude of maximum current drawn is almost 12 A whereas the magnitude of average current is nearly 5 A.

Two more important performance parameters of a power supply are line regulation and load regulation. Line regulation is the percentage change in the output voltage in response to a change in the input voltage whereas load regulation is the percentage change in the output voltage in response to a change in load current. Small percentage of line and load regulation means the power supply responds very well to the changes in the input voltage and the load current, maintaining the output voltage very close to the specified value. Below are the calculations for the simulated line and load regulations which are quite high because of the open loop circuitry. Without feedback controller, the circuit cannot monitor the output and make duty cycle adjustments to compensate for voltage changes at the output.

$$\text{Line Regulation} = \frac{V_{O(HIGH\_INPUT)} - V_{O(LOW\_INPUT)}}{V_{O(NOMINAL\_INPUT)}} * 100\% = \left| \frac{1.086V - 0.9321V}{1.0135V} \right| * 100\% = 15.19\%$$

$$\text{Load Regulation} = \frac{V_{O(FULL\_LOAD)} - V_{O(NO\_LOAD)}}{V_{O(FULL\_LOAD)}} * 100\% = \left| \frac{1.0135V - 1.327V}{1.0135V} \right| * 100\% = 30.93\%$$

Summary of the simulation results are shown in Table 4.2

<b>Parameter</b>	<b>Value</b>
Input Voltage	10.8 V to 13.2 V
Nominal Output Voltage	1.0135 V
Maximum Output Current	40.54 A
Output Voltage Ripple	0.1 mV <sub>P-P</sub>
Nominal Switching Frequency	500 kHz per phase
Output Load Regulation	30.93%
Output Line Regulation	15.19%
Efficiency at Full Load	69.50%

Table 4.2      Summary of Multiphase Multi-Interleave Buck Converter Simulation Results

## Chapter 5 Hardware Verification

### 5.1 Multiphase Multi-Interleave Buck Schematic

A schematic for the proposed Multiphase Multi-Interleave Buck Converter is drawn using the ExpressSCH schematic software from the Express PCB website [28]. For convenience, the schematic is broken down into three pages: PWM controller connection, MOSFET drivers connection, and the output stage connection. These are shown in Figures 5.1, 5.2 and 5.3 respectively. All resistors used in the schematics are of 1% tolerance and are in ohms. All capacitors used in the schematics are in micro Farads ( $\mu\text{F}$ ) and all inductors are in micro Henries ( $\mu\text{H}$ ). Ports are used to connect the same point in the circuit to avoid crisscrossing the wires on the schematics. For example, Port named CS1 is used to connect pin 1 of the controller and the positive side of the capacitor C3 in Figure 5.1. The final component layout is shown in Figure 5.4. One of the objectives of this thesis is to reduce the board size to a 50% of the previous proposed circuit along with meeting the other performance parameters. The need for doing so is the increasing power demand for future processors, otherwise it is estimated that VRM's will occupy 30% of a PC motherboard area.

The PCB layout plays a critical role in the performance in a high frequency switching power supply design. Following measurements have been taken to improve the performance and expedite the design.

- To take the full advantage of the ripple cancellation factor from multi-interleaving, the input capacitors have been placed before the junction

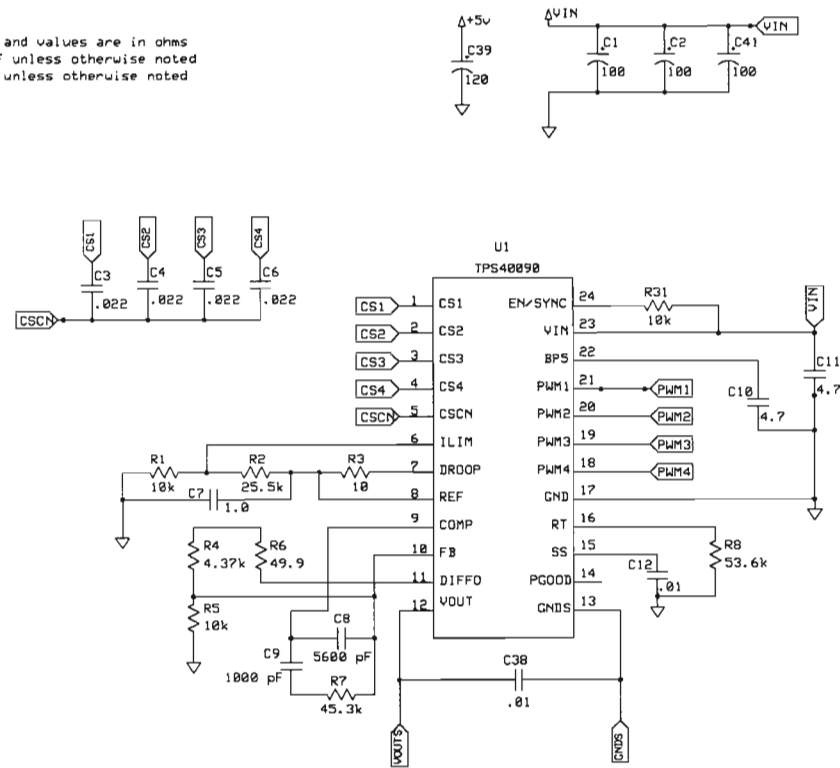
where the input voltage is distributed. Output capacitors have been placed after the junction where all the inductors are connected

- Placed the external drivers very near to the FET's and used thick trace for gate drive signal to improve noise immunity.
- Placed aluminum electrolytic capacitor in the input side to filter the current spikes.
- Placed enough vias along pads of the power components to increase thermal conduction.
- Kept the current sensing traces as short as possible to avoid excessive noise pick up.
- Placed the output inductors as symmetric as possible in relation to the output connectors to obtain similar voltage drop from the trace impedance.

The PCB board is laid out using ExpressPCB software [29]. The PCB board has four layers. Components are placed on the top layer. One inner layer is used as a ground plane, the other inner layer is used as power plane for 12V input and the bottom layer is used for multiple purposes such as for power plane for the 5Vsupply etc.. Details of each layer and layout are shown in Figures 5.5, 5.6, 5.7 and 5.8. Figure 5.9 shows the overall layout of the proposed converter's circuit. Table 5.1 shows the bill of materials.

**Notes:**

1. All resistor are 1% tolerance and values are in ohms
2. All capacitor values are in  $\mu\text{F}$  unless otherwise noted
3. All inductor values are in  $\mu\text{H}$  unless otherwise noted



**Cal Poly SLO**

**Multiphase Multi-Interleave Buck**

Furqan Saleemi

Rev 1.0

06/20/2008

PWM

Figure 5.1 Multiphase Multi-Interleave Buck Schematic Part I – TPS40090 Controller

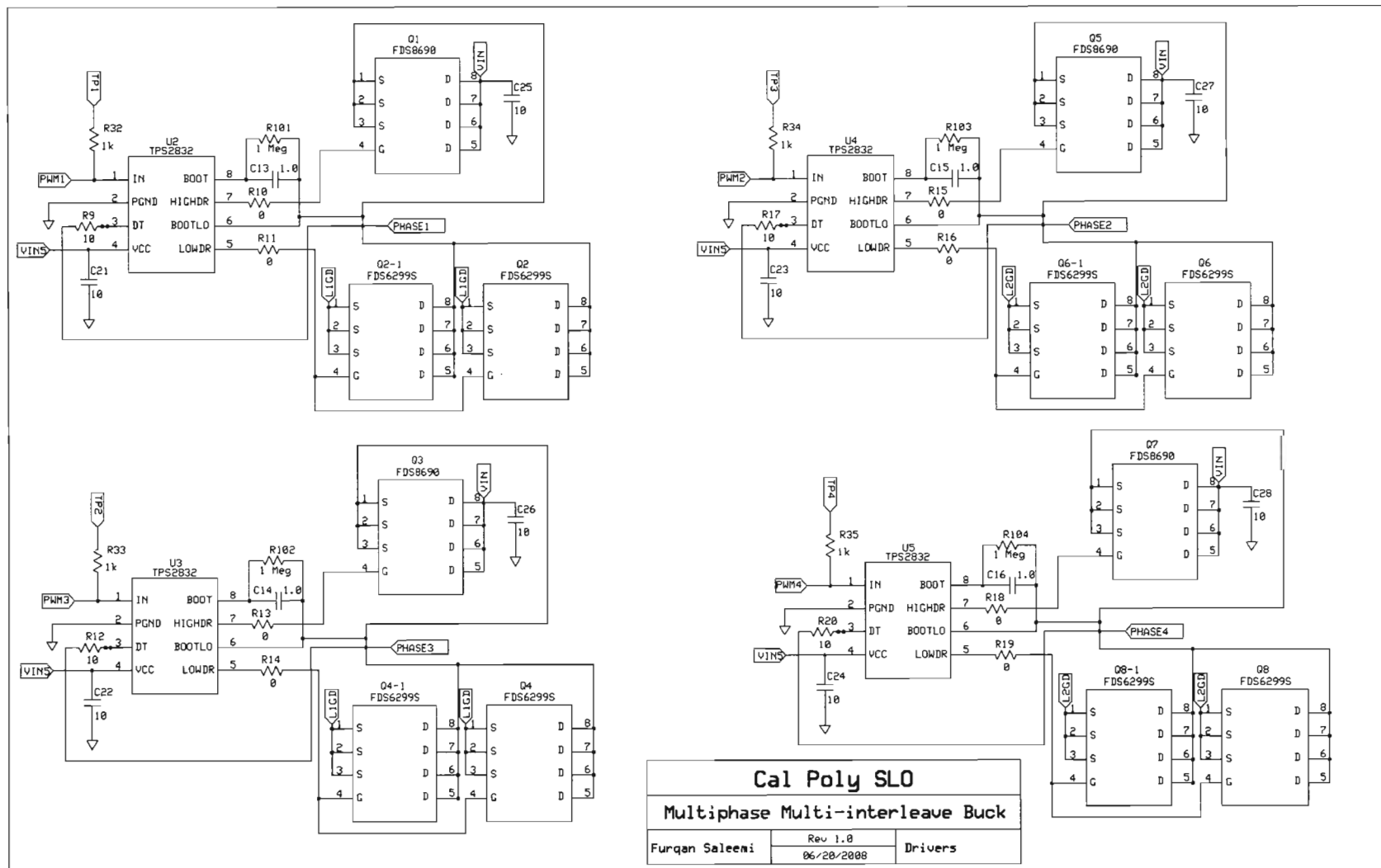


Figure 5.2 Multiphase Multi-Interleave Buck Schematic Part II – MOSFET Drivers

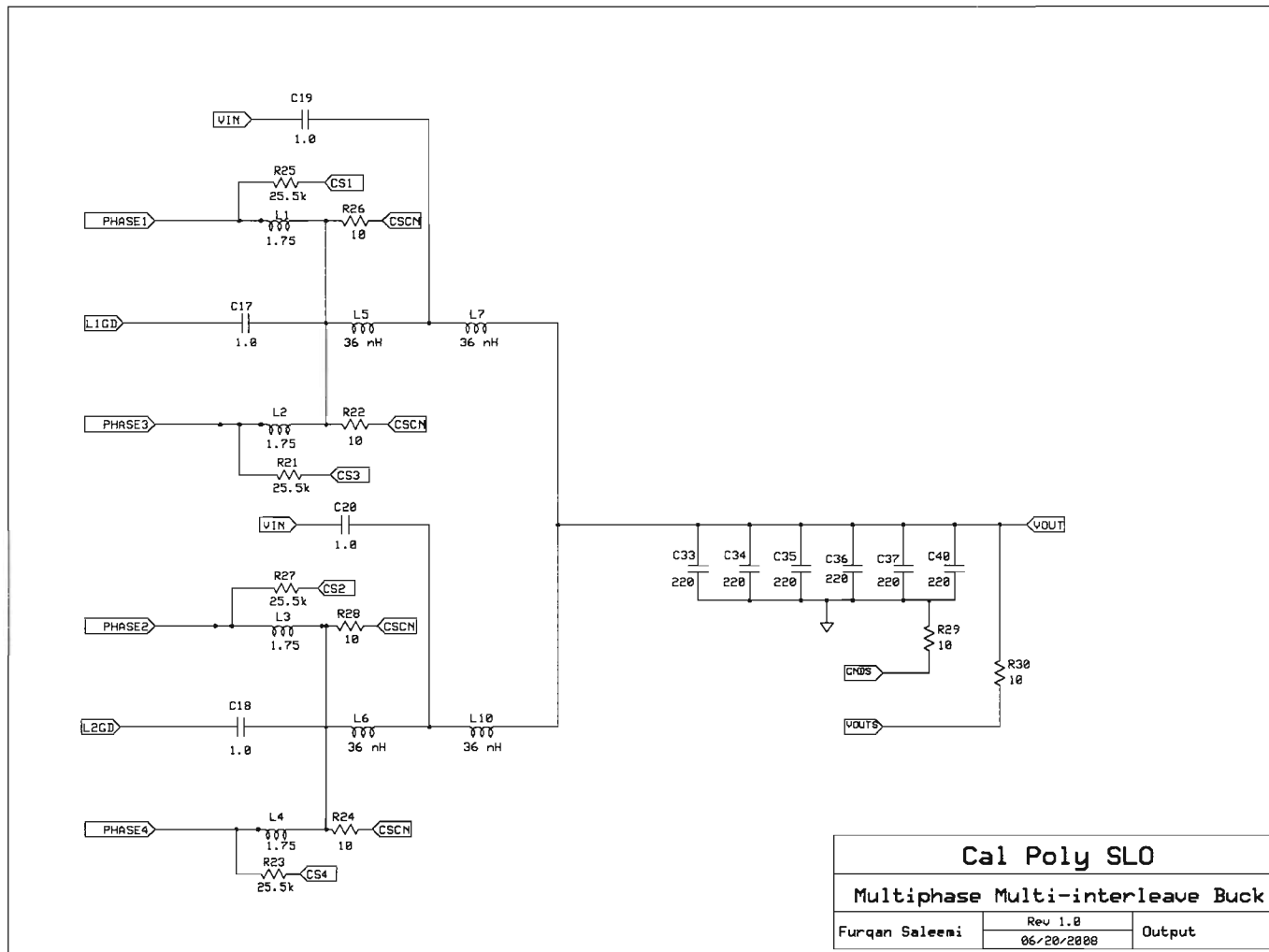


Figure 5.3 Multiphase Multi-Interleave Buck Schematic Part III – Power Stage

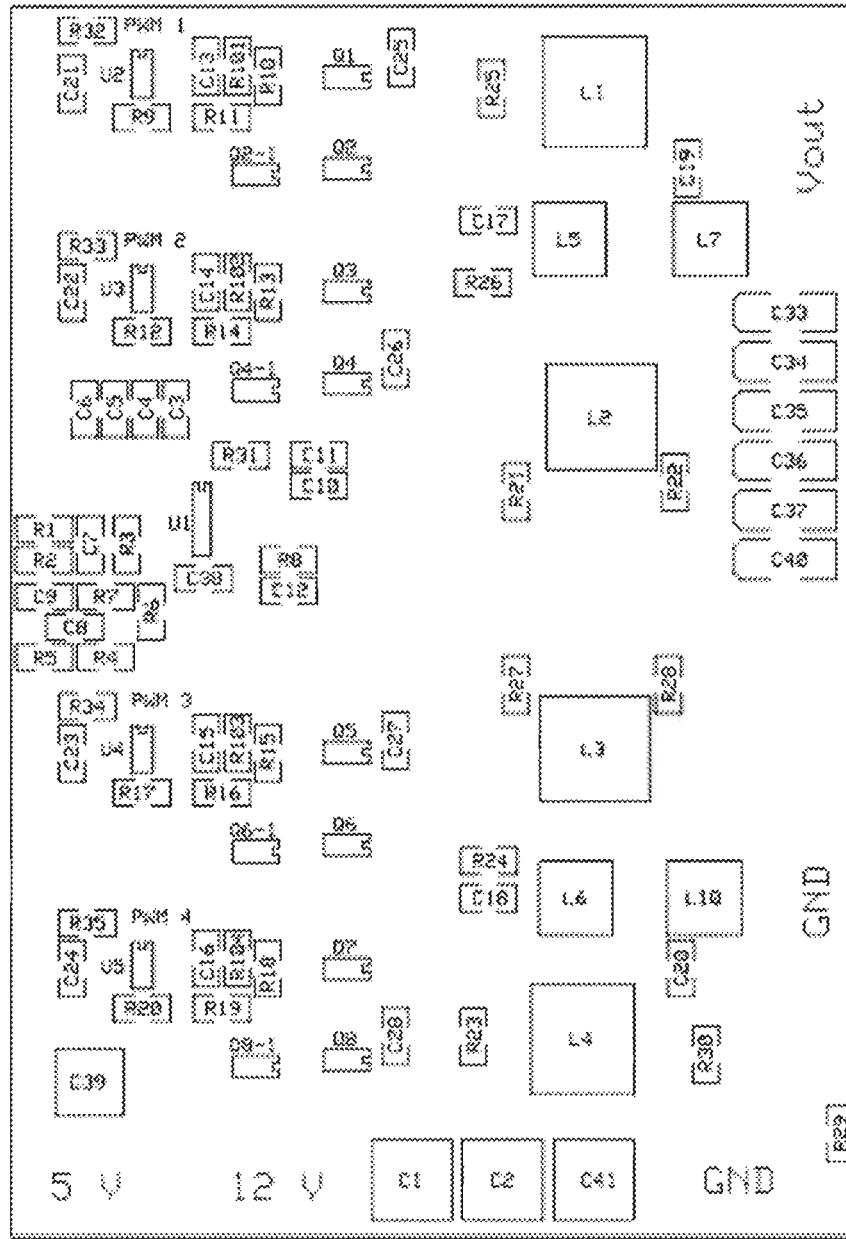


Figure 5.4 Multiphase Multi-Interleave Buck Components Layout



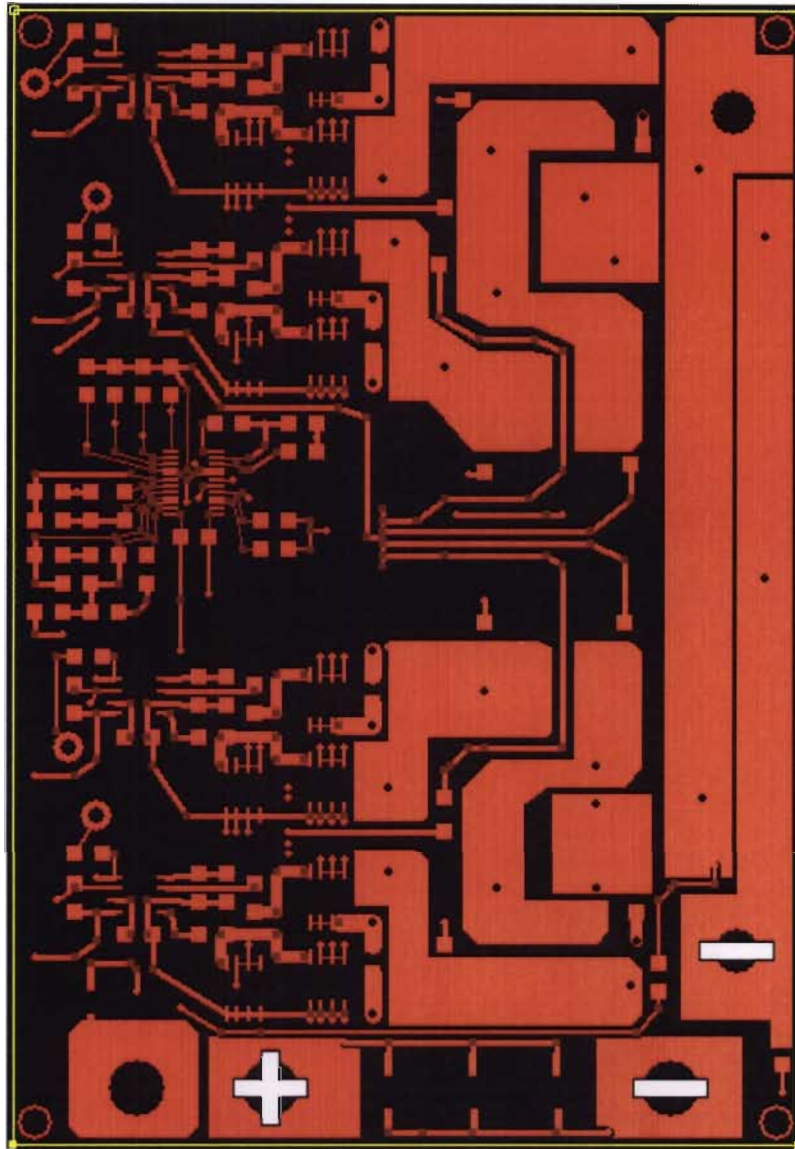


Figure 5.5 Top Copper Layer

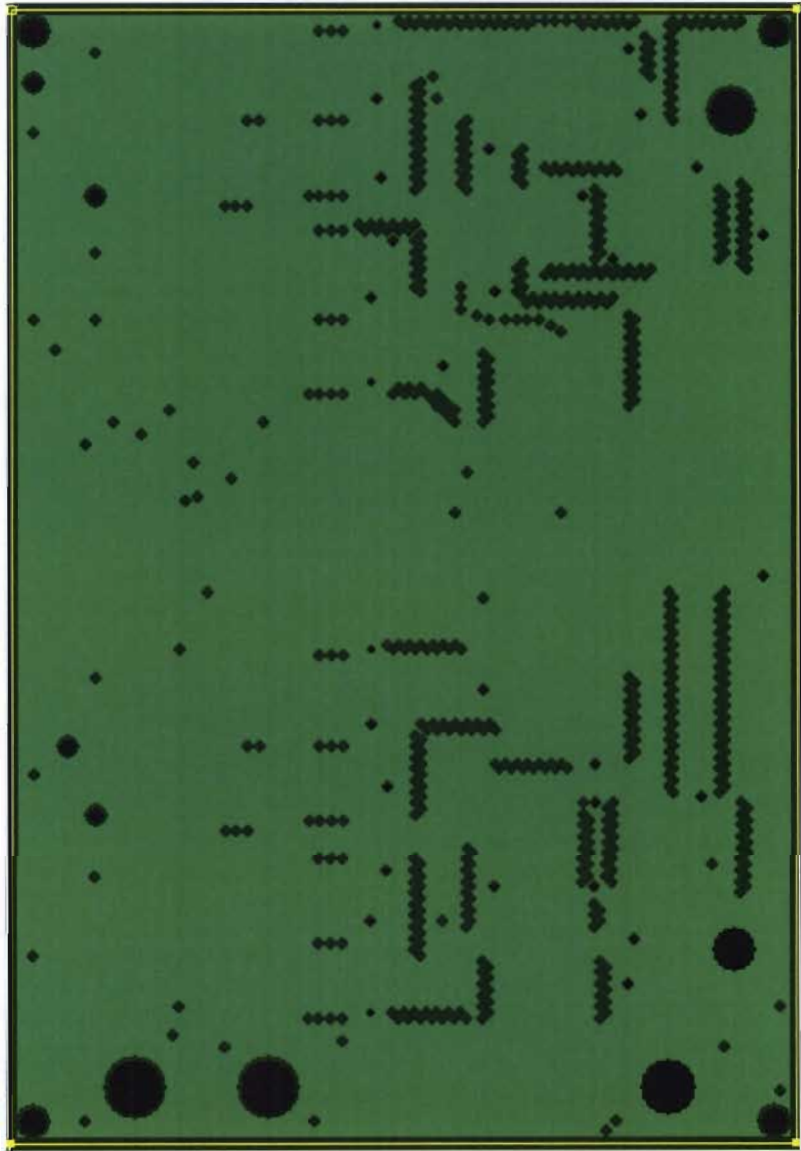


Figure 5.6 Ground Inner Layer

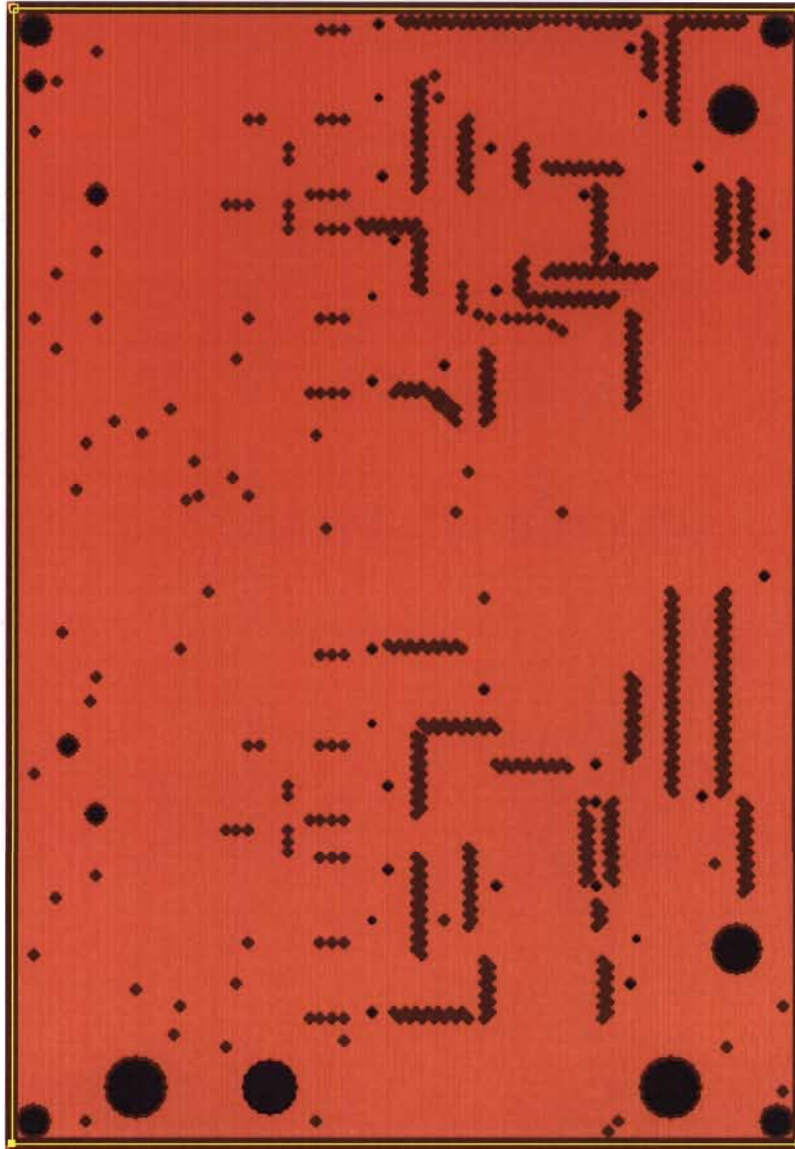


Figure 5.7 Power Inner Layer

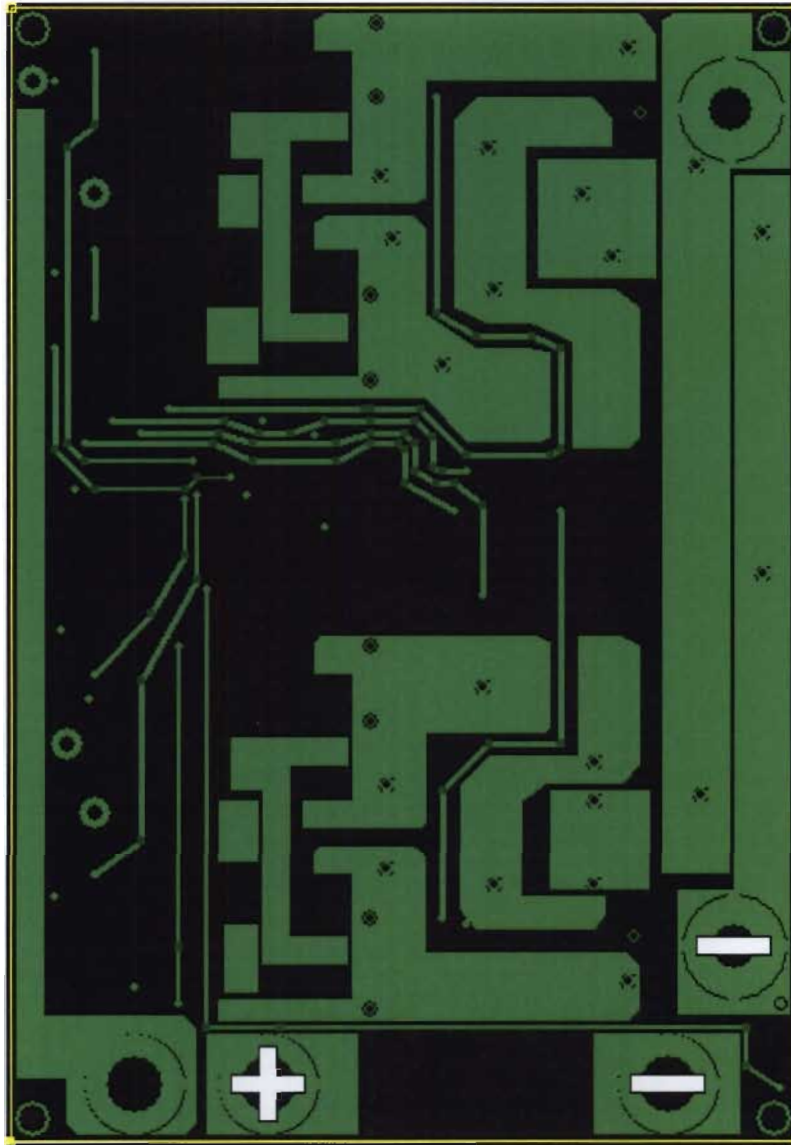


Figure 5.8 Bottom Copper Layer

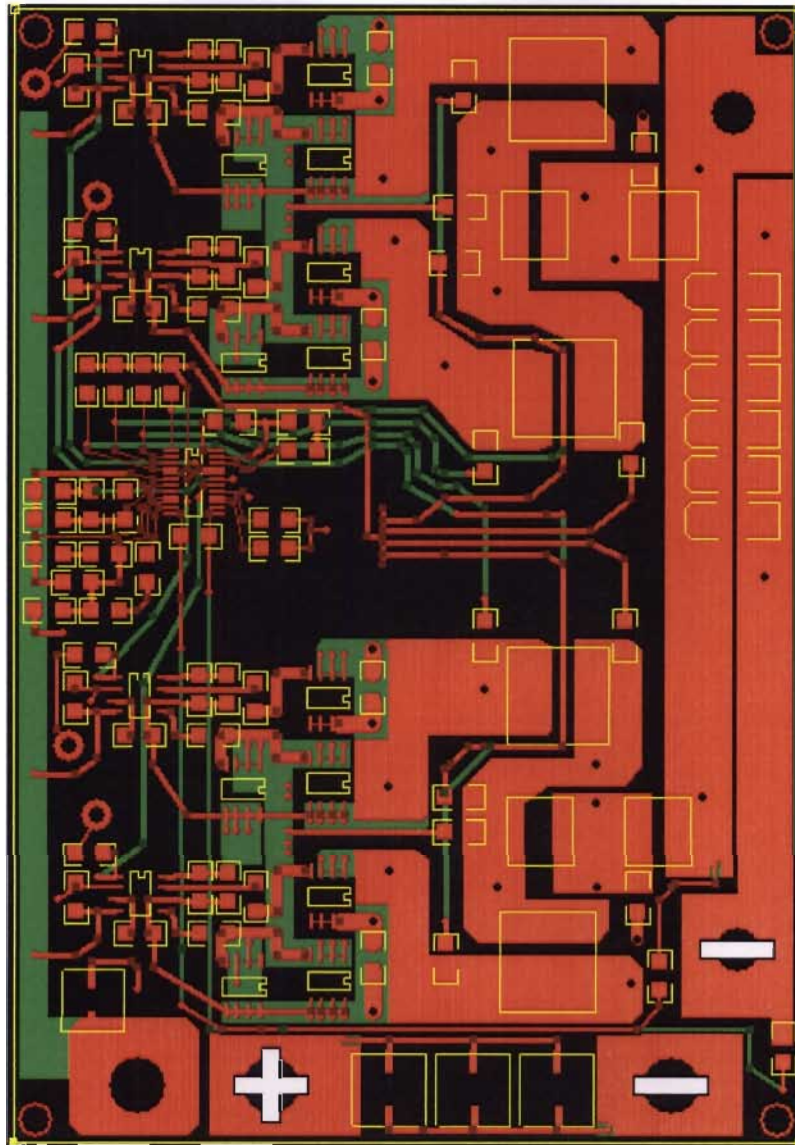


Figure 5.9 Overall Layout of the Circuit

Reference Designator	QTY	Description	Manufacturer	Part Number
C1,C2	2	Capacitor, Aluminum organic , 100uF,20V	Nichicon	94SVP107X0020E12
C39	1	Capacitor, Aluminum organic, 120uF,10V	Nichicon	PCJ1A121MCL1GS
C41	1	Capacitor, Aluminum elect. , 220uF,25V	Nichicon	UCD1E221MN1GS
C3 - C6	4	Capacitor, ceramic, SMT 1206, 0.022uF	Kemet	C1206C223K5RACTU
C7, C13 - C20	9	Capacitor, ceramic, SMT 1206, 1.0uF	Kemet	C1206C105K3RACTU
C8	1	Capacitor, ceramic, SMT 1206, 5600pF	Kemet	C1206C562K5RACTU
C9	1	Capacitor, ceramic, SMT 1206, 1000pF	Kemet	C1206C102K1RACTU
C10 -C11	2	Capacitor, ceramic, SMT 1206, 4.7uF	Kemet	C1206C475K3RACTU
C12, C38	2	Capacitor, ceramic, SMT 1206, 0.01uF	Kemet	C1206C103K1RACTU
C21 - C28	8	Capacitor, ceramic, SMT 1206, 10uF	Kemet	C1206C106K3PACTU
C33 -C37	6	Capacitor, Tantalum, SMT 7343, 220uF	Kemet	A700D227M002
L1 - L4	4	Inductor, SMT, 1.75uH	Coilcraft	MLC1260-172ML
L5 - L7, L10	4	Inductor, SMT, 36 nH	Coilcraft	SLC7649S-300KL
Q1 ,Q3,Q5, Q7	4	MOSFet, N-Channel, V, A	Fair Child	FDS8690
Q2,Q4,Q6,Q8	4			
Q2-1,Q4-1,Q6-1,Q8-1	4	MOSFet, N-Channel, V, A	ST	STS25NH3LL
R	4	Resistor, SMT 1206, 1 Meg , 1%	KOA Speer	RK73H2BTDD1004F
R1, R5, R31	3	Resistor, SMT 1206, 10k , 1%	KOA Speer	RK73H2BTDD1002F
R2, R21, R23, R25, R27	5	Resistor, SMT 1206, 25.5k , 1%	KOA Speer	RK73H2BTDD2552F
R3, R9, R12, R17, R20 R22, R24, R26, R28 - R30	11	Resistor, SMT 1206, 10 , 1%	KOA Speer	RK73H2BTDD10R0F
R4	1	Resistor, SMT 1206, 4.32k , 1%	KOA Speer	RK73H2BTDD4321F
R6	1	Resistor, SMT 1206, 49.9 , 1%	KOA Speer	RK73H2BTDD49R9F
R7	1	Resistor, SMT 1206, 45.3k , 1%	KOA Speer	RK73H2BTDD4532F
R8	1	Resistor, SMT 1206, 53.6k , 1%	KOA Speer	RK73H2BTDD5362F
R10, R11, R13 - R16, R18, R19	8	Resistor, SMT 1206, 0 , 1%	Vishay/Dale	CRCW12060000Z0EA
R32 - R35	4	Resistor, SMT 1206, 1k , 1%	KOA Speer	RK73H2BTDD1001F
U1	1	IC, high-frequency, multiphase controller	Texas Instruments	TPS40090
U2 - U5	4	IC, MOSFET driver, fast synchronous buck with DTC	Texas Instruments	TPS2832

Table 5.1 Bill of Materials

## 5.2 Test Setup

Figure 5.10 shows the top view of the converter whereas Figure 5.11 and 5.12 show the schematic and original test setup respectively. The green banana jack “1” is connected to 5 V power supply and red banana jack “2” is connected to 12 V power supply. Both input grounds connect to black banana jack “3”. Two electronic loads are connected in parallel to draw current up to full load of 40 A between  $V_{OUT}$  and GND, since a single electronic load is only able to draw up to 33 A due to low voltage protection. Leads which are being used for connecting the output of the circuit to the electronic loads should be as short as possible because of the voltage drop at higher load current. Voltage drop especially becomes an important issue when the output voltage is equal or less than 1V. Volt meter to read the output voltage is also placed in parallel with electronic loads. Figure 5.13 shows size comparison between new and previous converter. It is clear that the new printed circuit board is exactly half the size of the previous one with significant efficiency improvement, double the power density and better current sharing between the channels. The new printed circuit board has 3.5x5 inch physical dimensions and 17.5 inch<sup>2</sup> area. Table 5.2 shows the test equipment list used in the lab setup.



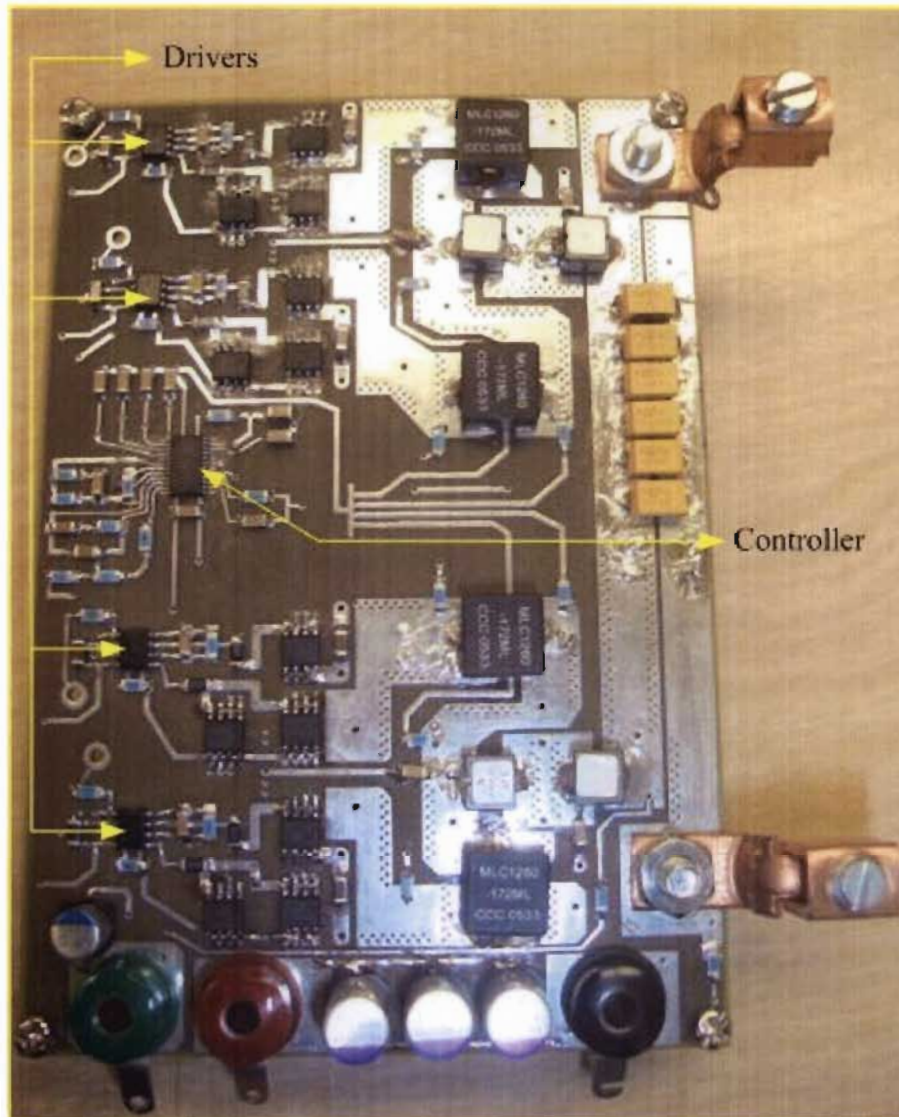


Figure 5.10 Top View of the Converter



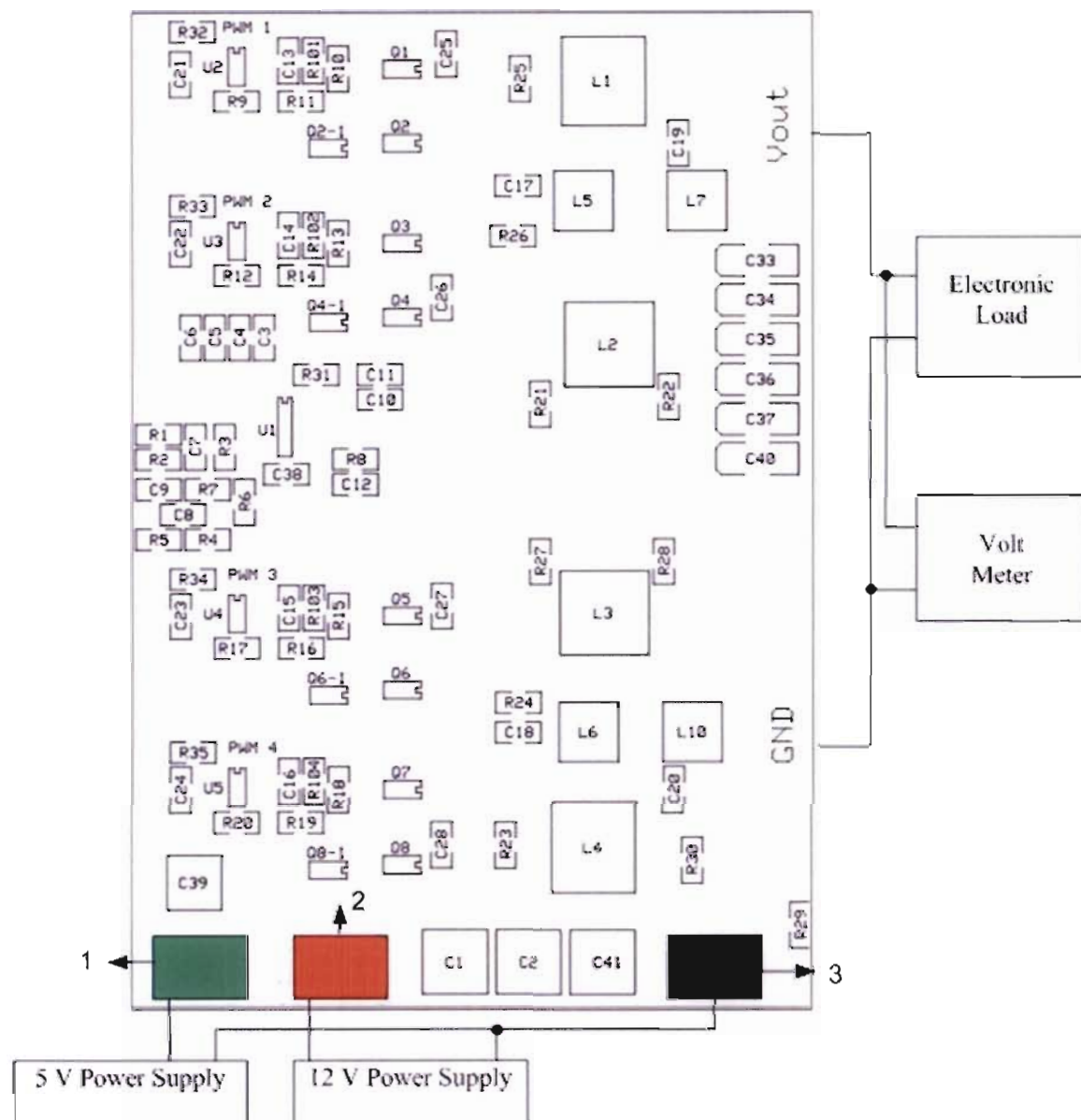


Figure 5.11 Test Setup Connections

Equipment	Description
Power Supplies	1. HP 6574A DC Power Supply 2. GW (GPR 6060D) Power Supply
Oscilloscope	1. GW Instek GDS 2204 Four Channel Digital Storage Oscilloscope 2. HP 54610B Oscilloscope
Multimeters	1. Instek Dual Display Digital Multimeter (GDM-8245) 2. Fluke 87 True RMS Multimeter
Load	1. HP 6060B System DC Electronic Load 2. Executive Engineering
Current Probe Amplifier	Tektronix TM502A Current Probe Amplifier
Current Probe	Tektronix A 6302 Current Probe

Table 5.2 Test Equipment List

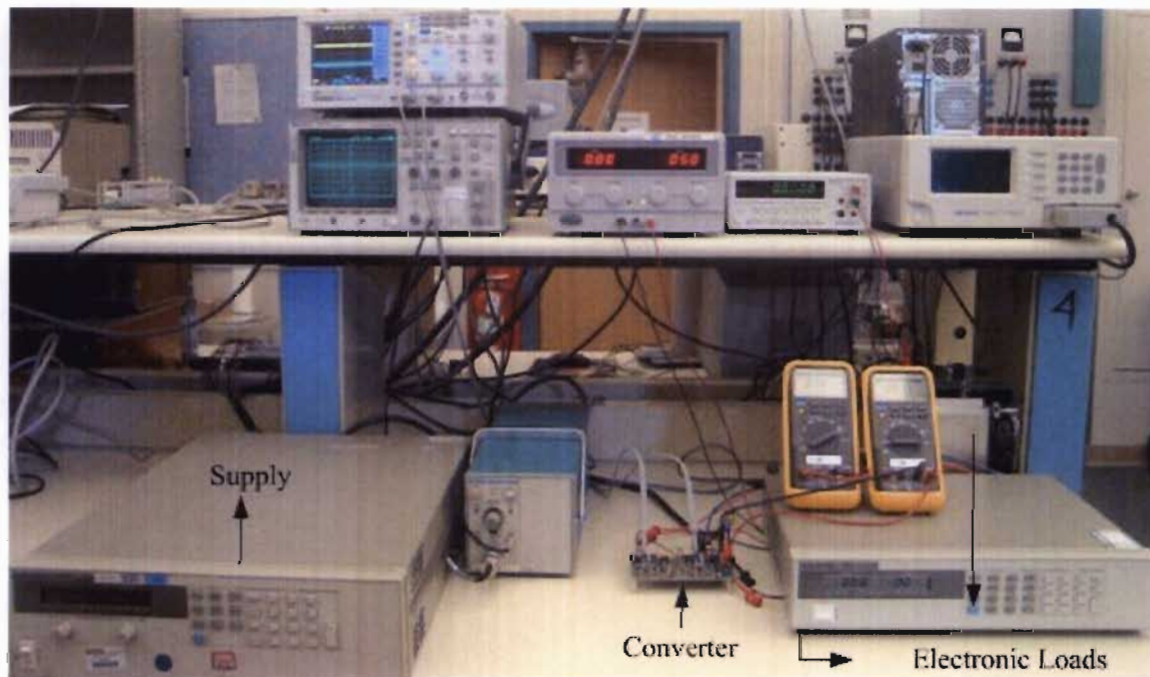


Figure 5.12 Photo of Test Setup

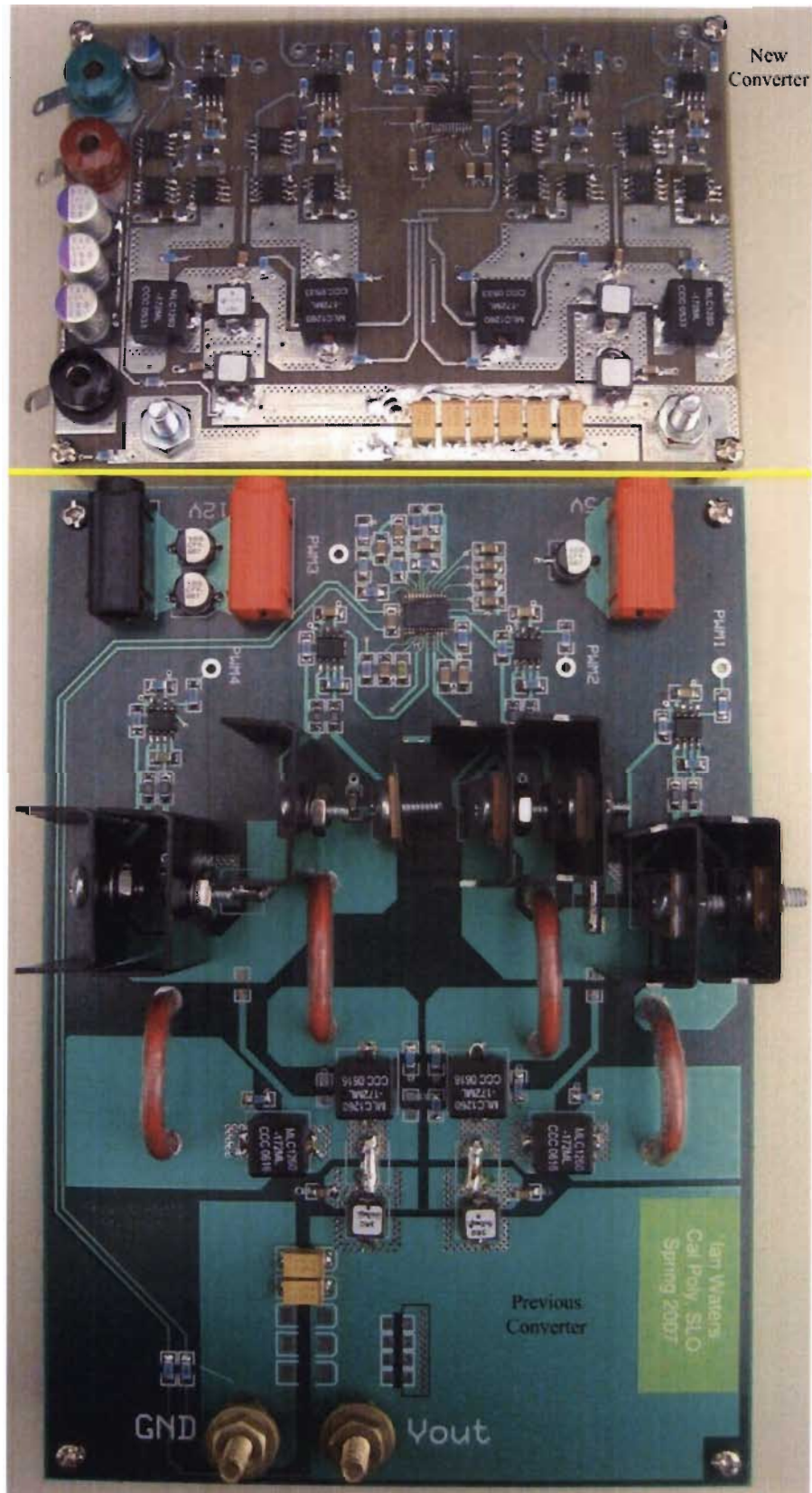


Figure 5.13 Size Comparison between New and Previous Converter

## 5.3 Test Results

### 5.3.1 PWM Outputs

As mentioned earlier that in multiphase multi-interleave buck the gate signals are  $90^\circ$  apart. In Figure 5.14, signals are represented according to the phases drawn in the circuit. PWM 1 waveform is phase 1 which is  $90^\circ$  apart from the PWM 2 waveform which represents phase 2. PWM 3 waveform of phase 3 is  $90^\circ$  apart from the phase 2 but  $180^\circ$  from phase 1. The PWM 4 waveform is phase 4 which is  $90^\circ$  apart from phase 3,  $180^\circ$  from phase 2 and  $270^\circ$  from phase 1. With the time scale set at 500 ns/div, the operation frequency of each phase is 494.3 kHz.

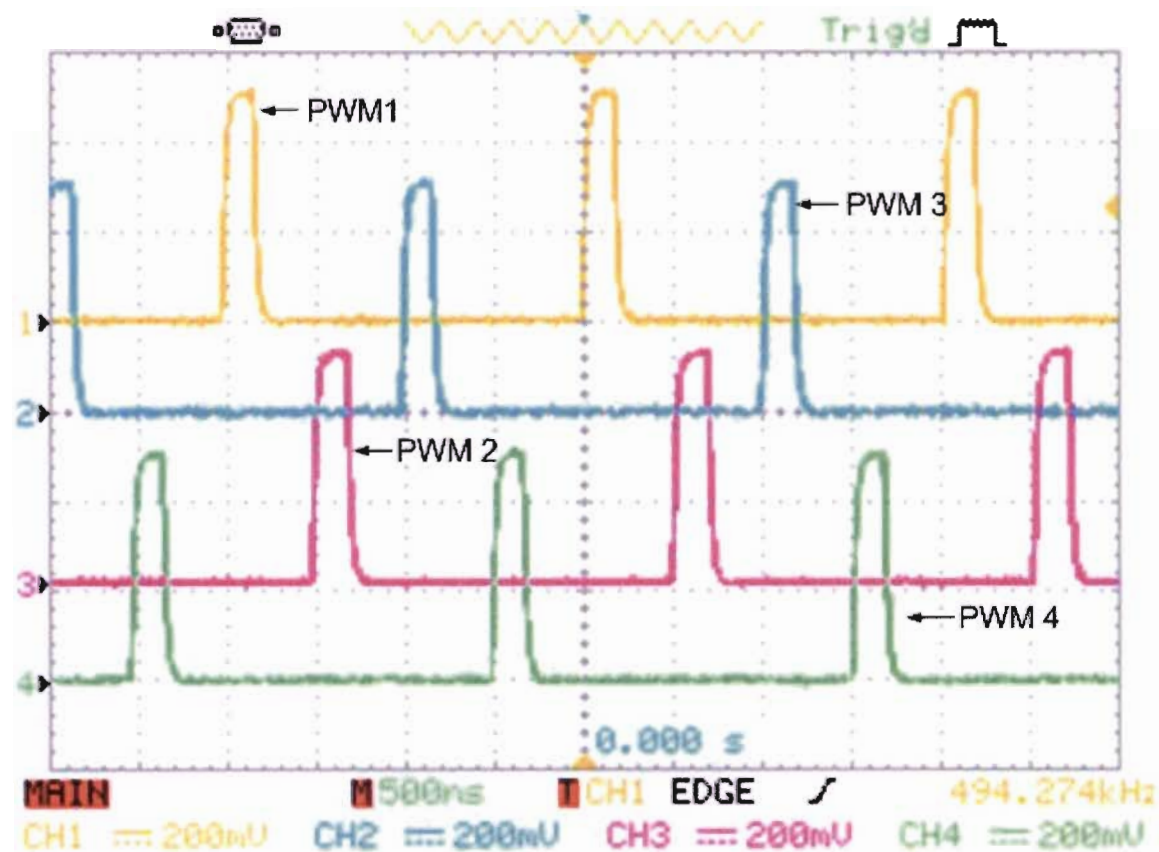


Figure 5.14 PWM Outputs at the Controller



### 5.3.2 Output Voltage Ripple

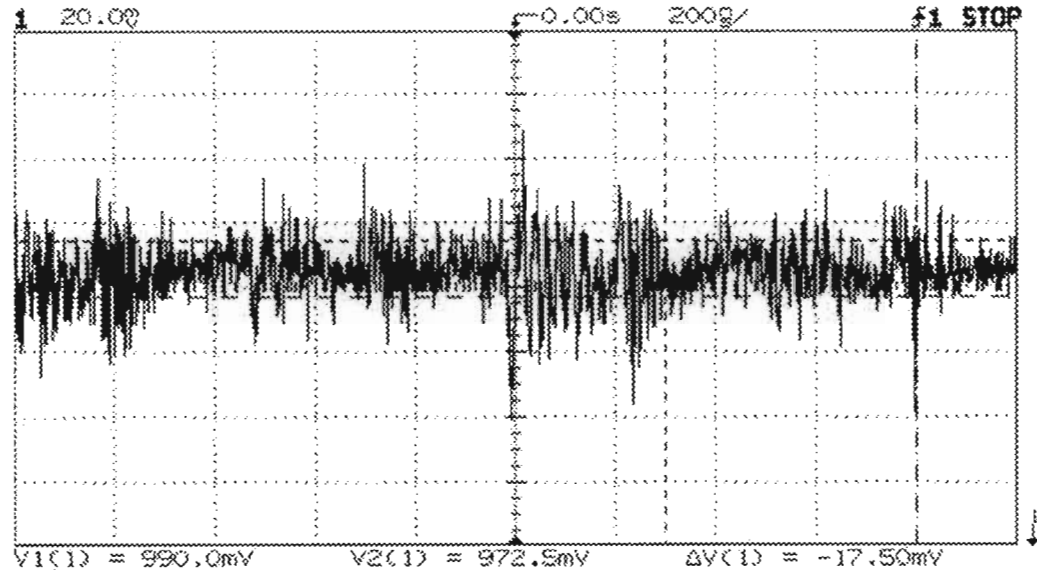


Figure 5.15 Output Voltage Ripple Waveform

Output voltage ripple is an important performance criterion. For the proposed topology, the ripple is shown in Figure 5.15 and was measured to be 17.50 mV when  $V_{IN} = 12$  V and  $I_O = 35$  A, which meets the requirement of 50 mV and smaller than the set parameter value. Figure 5.16 shows the ripple frequency ( $\frac{1}{\Delta t}$ ) of the output voltage which is exactly 2 MHz.

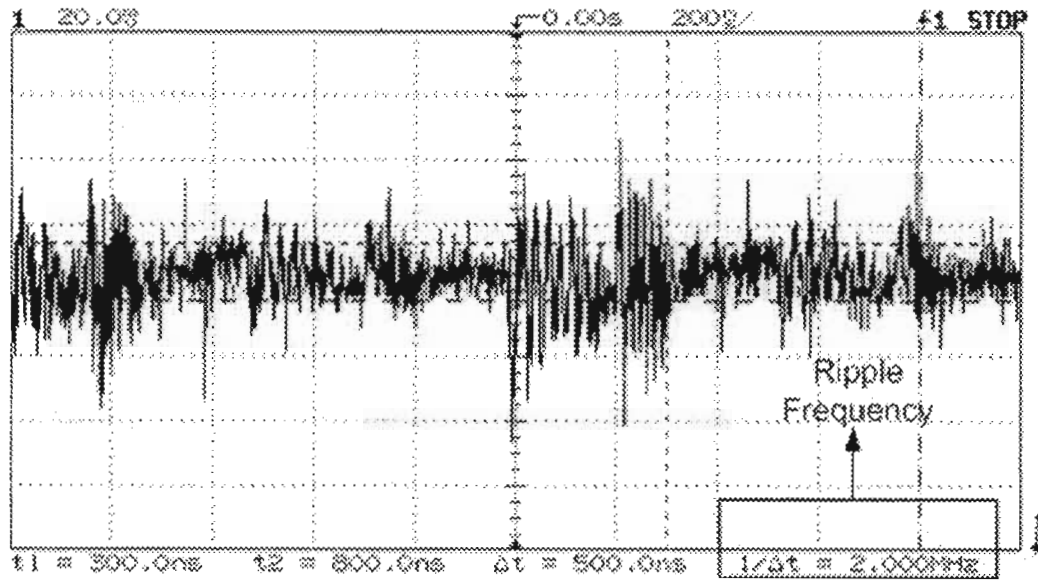


Figure 5.16 Frequency of Output Voltage Ripple

### 5.3.3 Current Sharing

In this multiphase multi-interleave buck converter circuit, no current measurement jumpers have been used to reduce the board area and increase the efficiency. So to check the current sharing, the Volt Second Area concept which states that “In steady state the average inductor voltage is zero over one switching period” has been used. This means the change in inductor voltage during charging or on time would be same as that of during discharging or off time. Due to the non-availability of jumpers and limitations on oscilloscope, the voltage on both sides of output inductor of each phase has been measured and by using the math function the difference has been calculated and plotted. Figures 5.17, 5.18, 5.19, and 5.20 show the inductor voltage during on and off time of phase 1, phase 2, phase 3 and phase 4 respectively.

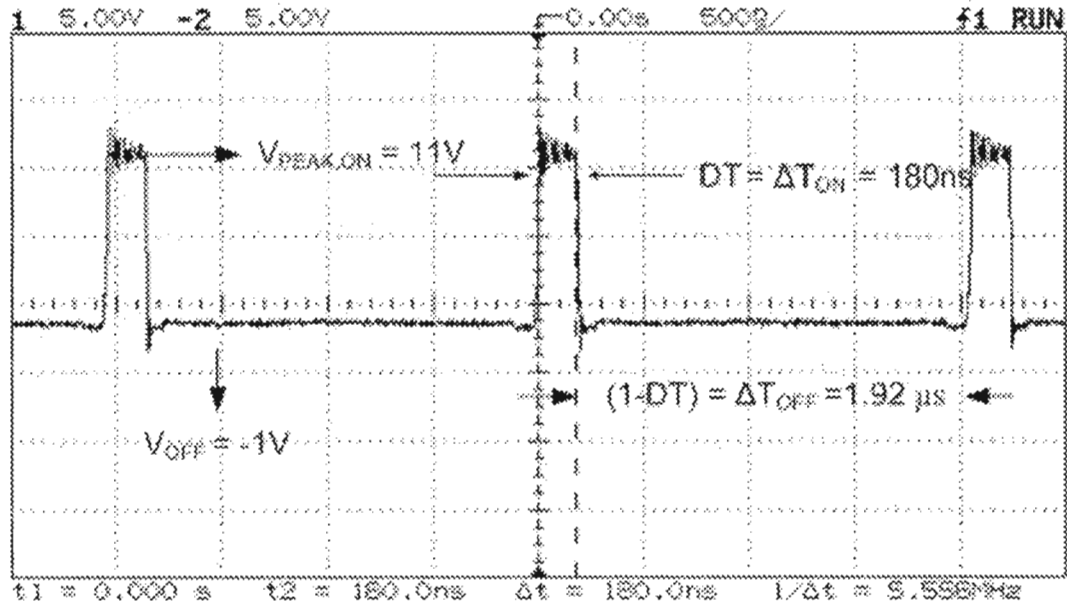


Figure 5.17 Voltage Across L1 Inductor During Charging and Discharging Time

Furthermore Figure 5.17 shows that charging time is 180 ns, which is almost equal to the time of duty cycle of 166 ns. Also in Figure 5.18 one full switching period is shown which has a frequency of 497.5 kHz which is very close to the designed frequency of 500 kHz.

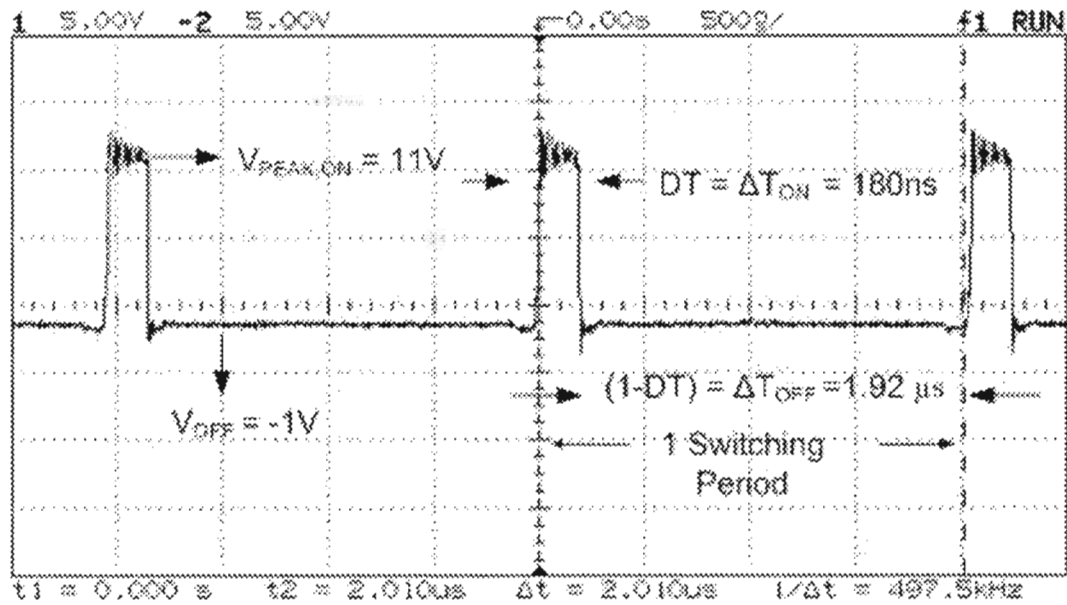


Figure 5.18 Voltage Across L3 Inductor During Charging and Discharging Time

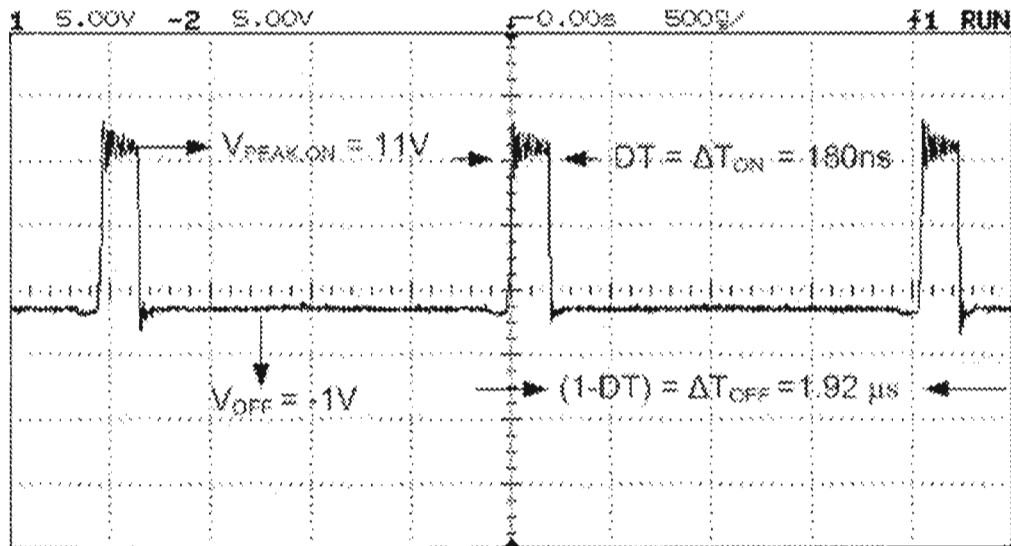


Figure 5.19 Voltage Across L2 Inductor During Charging and Discharging Time

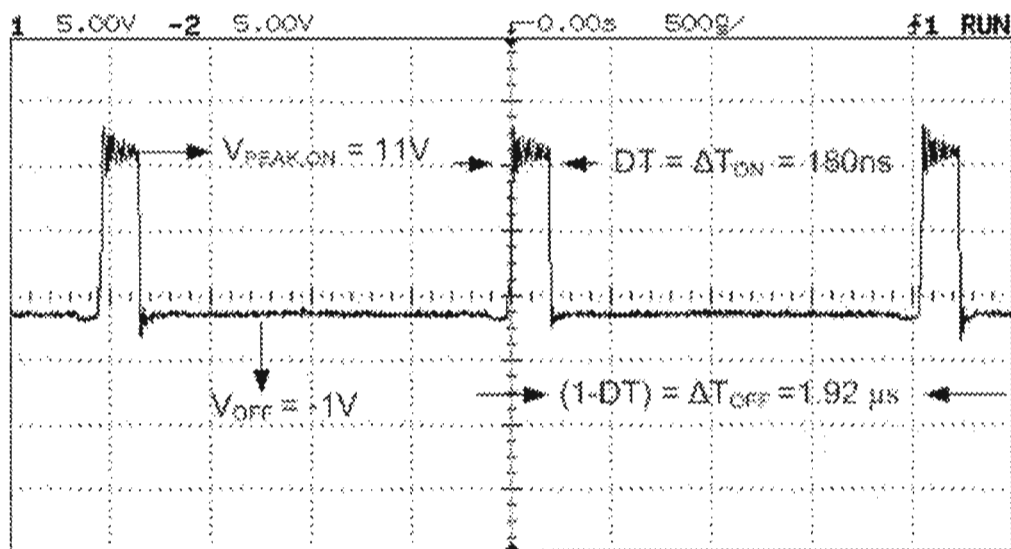


Figure 5.20 Voltage Across L4 Inductor During Charging and Discharging Time

With  $V_{IN}$  12 V and  $V_O$  is 1 volt, the previous oscilloscope plots confirm that for each phase, during charging or on time the inductor voltage is 11 V, while during discharging or off time the inductor voltage is -1 V. As all four phases show the same plots with exact same voltages across the inductor during both on and off time, we can then conclude that the equal current sharing achieved. In Figure 5.21 the inductor current



has been shown with average inductor current per phase. Due to unavailability of jumper, inductor current ripple has been calculated and drawn.

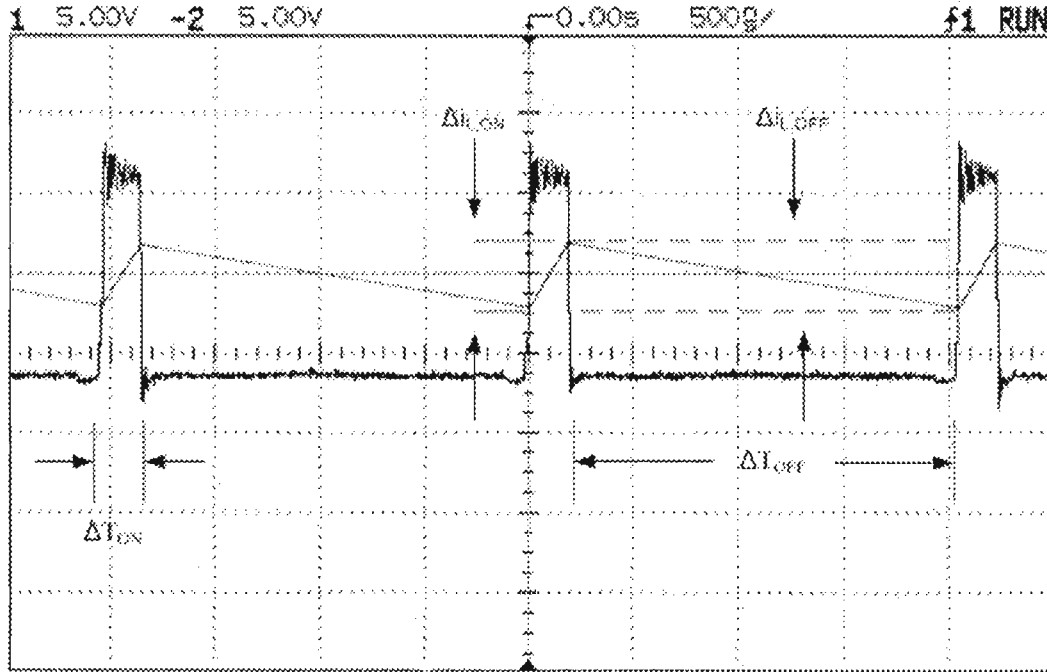


Figure 5.21 Inductor Current Ripple and Average Inductor Current per Phase

The following calculation shows how the inductor current ripple is deduced from the inductor voltage:

$$V_L = L \frac{di}{dt} \quad \text{Equation 5.1}$$

$$di = \frac{V_L}{L} (dt) \quad \text{Equation 5.2}$$

which can be rewritten as:

$$\Delta i = \frac{V_L}{L} (\Delta t) \quad \text{Equation 5.3}$$

For on time  $V_L = V_{IN} - V_O$  and  $\Delta t = DT$

For off time  $V_L = -V_O$  and  $\Delta t = (1 - D)T$

Thus,

$$\Delta i = \frac{V_{IN} - V_o}{L} (DT) = -\frac{V_o}{L} (1 - D)T$$

$$\Rightarrow R.H.S = \frac{V_{IN} - V_o}{L} (DT) \text{ and } L.H.S = -\frac{V_o}{L} (1 - D)T$$

where from Figure 5.17 for  $L_1$ :

$$V_{IN} = 12V$$

$$V_o = 1V$$

$$L = 1.75 \times 10^{-6} H$$

$$DT = 180 nsec$$

$$(1 - D)T = 1.92 \times 10^{-6} sec$$

$$R.H.S = 1.13A \text{ and } L.H.S = 1.09A$$

$$\Rightarrow \Delta i = R.H.S \approx L.H.S$$

During the test for current sharing, output current  $I_o$  was 20 A, which means 5 A was contributed from each phase. The calculations for the other three phases ( $L_3$ ,  $L_2$  and  $L_4$ ) are exactly the same as indicated by Figures 5.18, 5.19 and 5.20. The calculated ripple is found to be less than the simulated ripple as shown in Figure 4.6.

### 5.3.4 Transient Response

Transient response is basically the measure of how output voltage responds to the change in the load from light to heavy and heavy to light load. A 0 to 20 A step up and 20 A to 0 step down change were used for the test. The full load transient response is not available because of current probe limitation. Figure 5.22 shows the change in output voltage when load is stepped down from 20 A to 0. The output voltage changes about 58 mV. Figure 5.23 depicts that the settling time for the transient is approximately 138  $\mu s$ .

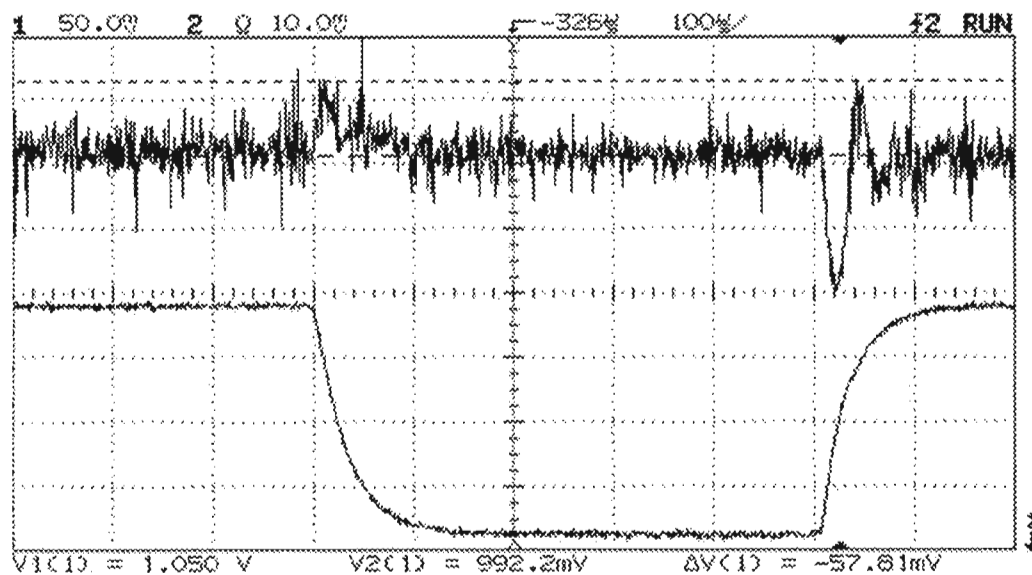


Figure 5.22 Output Voltage Transient Overshoot (20A to 0)

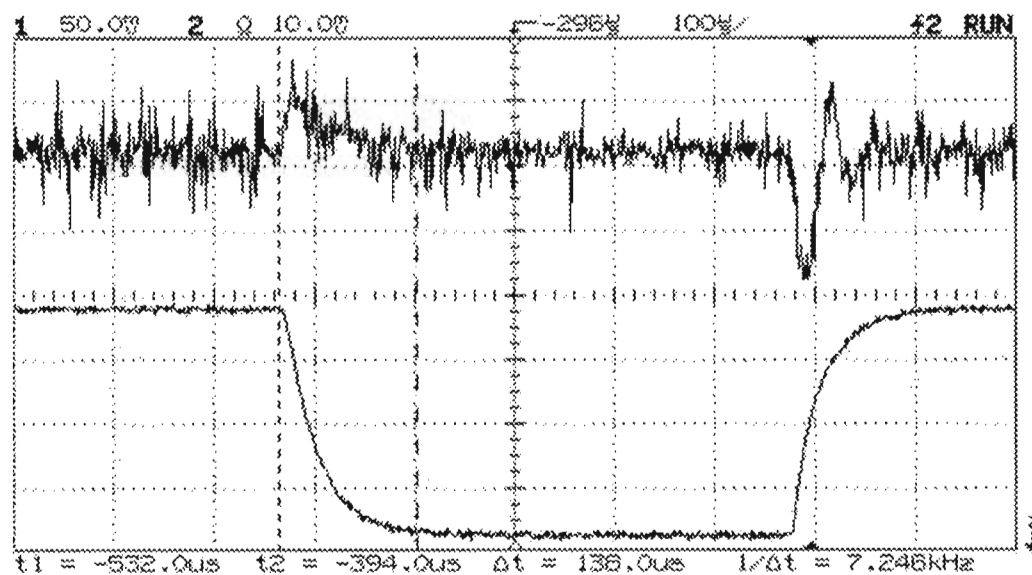


Figure 5.23 Output Voltage Transient Settling Time (20A to 0)

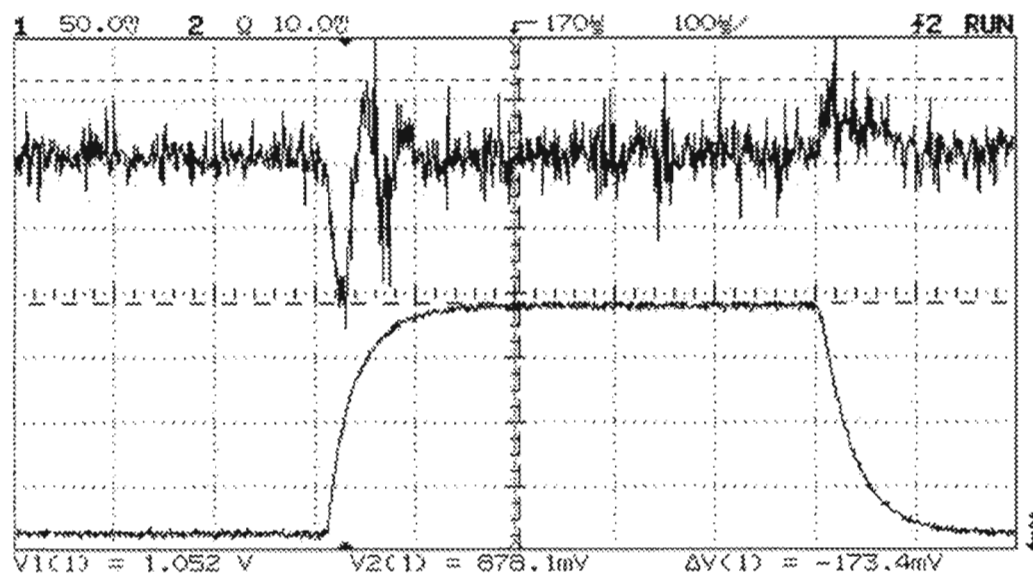


Figure 5.24 Output Voltage Transient Overshoot (0 to 20A)

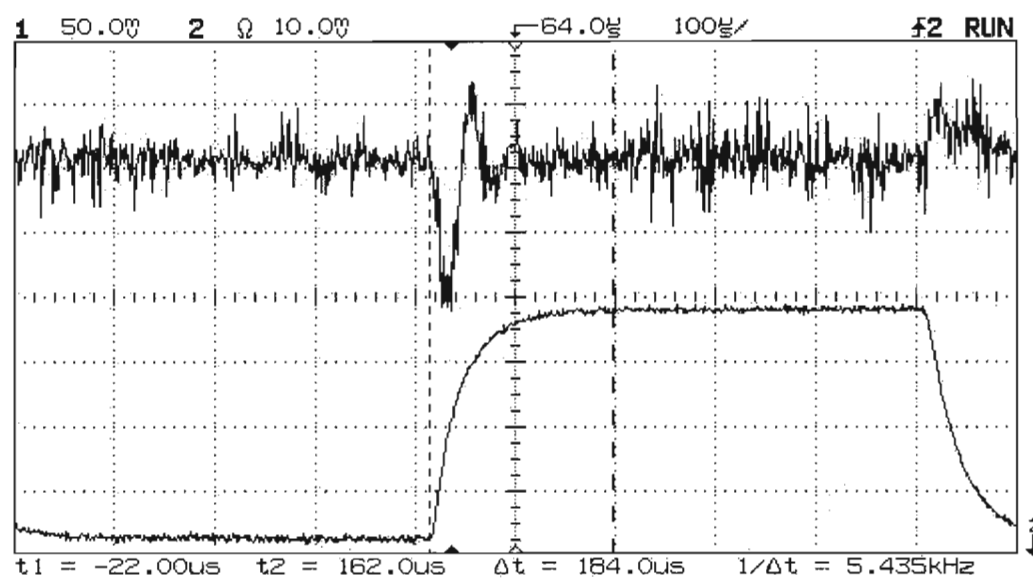


Figure 5.25 Output Voltage Transient Settling Time (0 to 20A)

Figure 5.24 shows the change in the output voltage when the load current is stepped up from 0 to 20 A. The figure shows that the change is about 173.4 mV. Figure 5.25 shows the settling time which is 184  $\mu\text{s}$  with the slew rate of 5A/ $\mu\text{s}$ .

### 5.3.5 Efficiency, Power Loss and Regulations

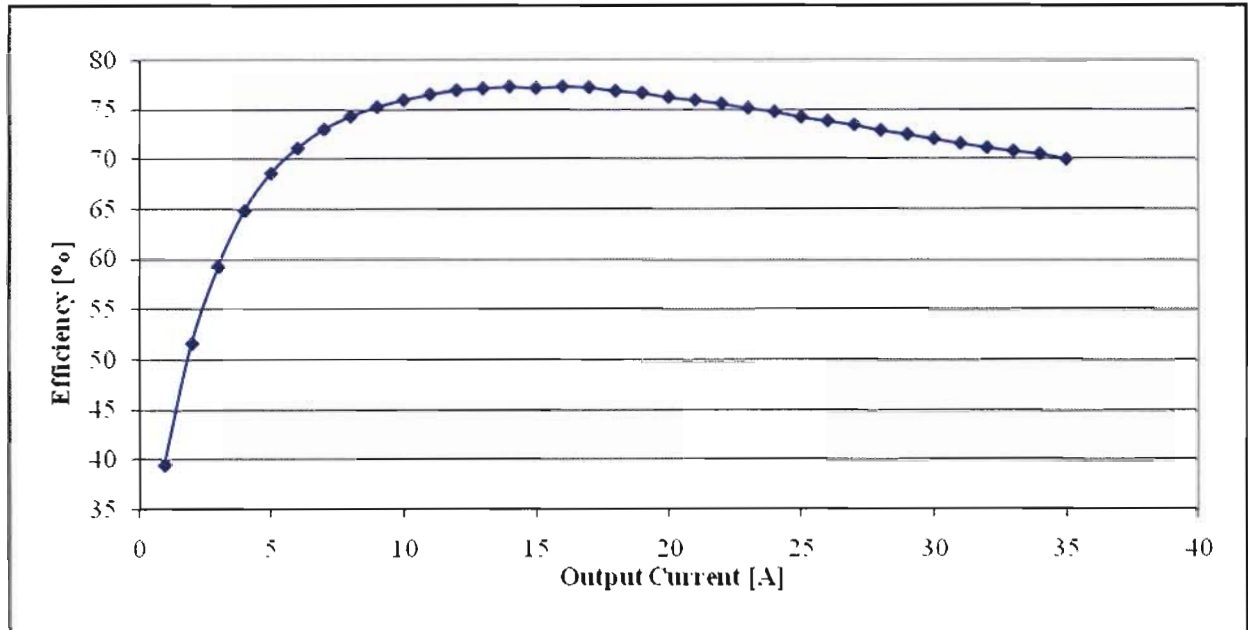


Figure 5.26 Overall Efficiency vs. Output Current

Another important performance parameter of the power supply is its overall efficiency. In Figure 5.26, the overall efficiency of the circuit is plotted against the output current. The output current is varied from 1 A to 35 A with efficiency of 70% at 35 A and maximum of 77.4% at 16 A which is 40% of full load. Circuit is tested at less than the maximum designed load due to poor heat dissipation on phase 1. Circuit has been tested at full load once using STS25NH3LL as the bottom switch in place of FDS6299S. Efficiency plot and complete data for both bottom MOSFETs are included in Appendix. Figure 5.27 shows the trend between load current and power losses in the circuit. The plot shows a general trend that power losses in the circuit increase with the increase in the output current.

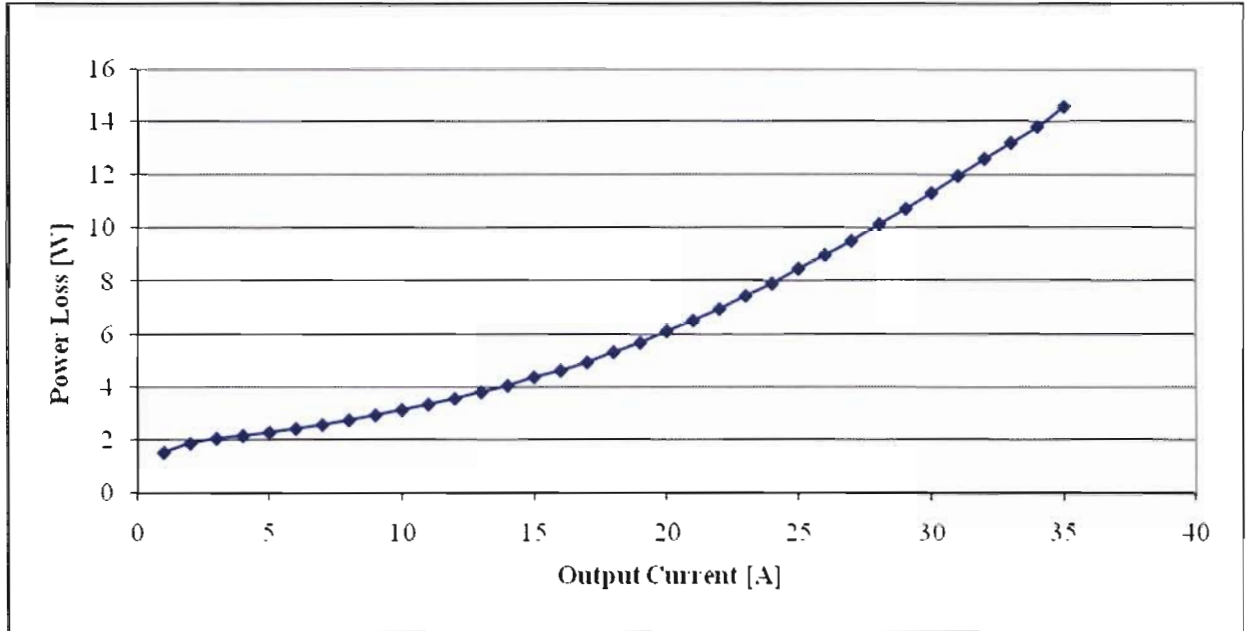


Figure 5.27 Power Loss vs. Output Current.

Due to the addition of feedback circuit, the converter's load regulation and line regulation has been greatly reduced as compared to simulated results. Load regulation is measured to be 3.559% while the line regulation is 0.144%. Calculations for both parameters are shown below.

$V_{IN}$ [V]	$V_{OUT}$ [V]	$I_{OUT}$ [A]
12.0	1.006	0
12.0	0.970	35
10.8	0.971	35
13.2	0.969	35

Table 5.3 Data for Calculating Load Regulation and Line Regulation

$$\text{Load Regulation} = \frac{V_{O(FULL\_LOAD)} - V_{O(NO\_LOAD)}}{V_{O(NO\_LOAD)}} * 100\% = \left| \frac{0.9701 - 1.0059}{1.0059} \right| * 100 = 3.559\%$$

$$\text{Line Regulation} = \frac{V_{O(HIGH\_INPUT)} - V_{O(LOW\_INPUT)}}{V_{O(NOMINAL\_INPUT)}} * 100\% = \left| \frac{0.9694 - 0.9708}{0.9701} \right| * 100 = 0.144\%$$

## Chapter 6 Summary and Future Work

According to Moore's law, the number of transistors in a computer doubles every two years. Increase in the number of transistors means more power consumption. According to International Technology Roadmap for Semiconductors, the requirement for power is increasing by 10W per year since 2001 for high performance CPU. To reduce the power losses the power supply voltage will be around 0.7 V and the current demand will be 170A in year 2010. Another challenge is to increase the power density since otherwise power regulator module is estimated to occupy 30% of a PC motherboard area due to the power requirements of future microprocessors.

With the VRMs topology of synchronous buck, serious technical challenges contribute to decreased power density and increased cost. These technical challenges are: 1) very small duty cycle, 2) high switching frequencies, and 3) higher current demands. Very small duty cycle ( $< 0.1$ ) contributes to slow transient response and low overall efficiency. Higher switching frequency causes more power dissipation and decreases efficiency. With higher current demands, more input and output capacitors are required to reduce the ripple current.

A Multiphase Multi-Interleave buck topology is proposed to solve the above technical challenges. Based on Intel's VRM 9.1 guidelines, design specifications for the voltage regulator module were determined. Using the theoretical calculations, values of important parameters like inductors, output capacitors and switches were found. To simulate the module, Orcad Pspice is used and the printed circuit board was designed by using PCB Express. After the simulation and design of PCB, the prototype was built. The board performed very well and met most of the specifications and goals. Table 6.1 shows

the summary of the proposed converter's performance parameters which are achieved, partially achieved or not achieved. In comparison to previous converter, the proposed new multi-interleaving converter has successfully doubled the power density. The size of the board has been reduced to half as that of the previous one. The new voltage regulator module shows the efficiency improvement of 15% and an increase from 55% to 70% at full load. Though the target of 80% efficiency has not been achieved yet, however the load regulation is 1.6 % above the set target.

Performance Parameter	Achieved or Not
Output Voltage	Achieved
Output Current	Partially Achieved
Output Voltage Ripple	Achieved
Switching Frequency	Achieved
Power Density	Achieved
Line Regulation	Achieved
Load Regulation	Not Achieved
Efficiency	Not Achieved but significantly improved

Table 6.1 Summary of the Achieved and Not Achieved Performance Parameters

For future work a better lay out can be planned to resolve the poor heat dissipation such that the circuit can be designed for a full load of 150 A to meet the real world need. One of the drawbacks of using synchronous buck as a basic building block of a multiphase multi-interleave converter is its bad input current characteristics. Though in multiphase multi-interleave converter, the peak of the input current is significantly reduced but it still have pulsing waveform with pulse widths of  $\frac{V_o}{V_{IN}}$ . There is a margin of improving the input current characteristics in future and make it as close to the dc current as possible. Furthermore work can be done on improving the efficiency and load regulation by selecting more appropriate and less resistive components. New digital



controllers and better drivers are another area to explore and integrate with this topology of multi-interleaving to improve the overall performance of the circuit.

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# APPENDIX

## Efficiency (Experimental Data with FDS6299S as a Bottom Switch)

Drivers		System				Calculations			
$V_{IN(D)}$ [V]	$I_{IN(D)}$ [A]	$V_{IN}$ [V]	$I_{IN}$ [A]	$V_O$ [V]	$I_O$ [A]	$P_{IN}$ [W]	$P_{OUT}$ [W]	$P_{LOSS}$ [W]	Efficiency [%]
5	0.130	12	0.062	1.006	0	1.394			
5	0.120	12	0.162	1.005	1	2.544	1.005	1.539	39.501
5	0.120	12	0.274	1.004	2	3.888	2.008	1.880	51.641
5	0.120	12	0.373	1.003	3	5.076	3.009	2.067	59.279
5	0.120	12	0.465	1.002	4	6.180	4.008	2.172	64.854
5	0.120	12	0.558	1.001	5	7.296	5.005	2.291	68.599
5	0.120	12	0.653	1.000	6	8.436	6.000	2.436	71.124
5	0.120	12	0.748	0.999	7	9.576	6.993	2.583	73.026
5	0.120	12	0.845	0.998	8	10.740	7.984	2.756	74.339
5	0.120	12	0.943	0.997	9	11.916	8.972	2.944	75.295
5	0.120	12	1.042	0.996	10	13.104	9.960	3.144	76.007
5	0.120	12	1.141	0.995	11	14.292	10.944	3.348	76.574
5	0.120	12	1.241	0.994	12	15.492	11.927	3.565	76.987
5	0.120	12	1.344	0.993	13	16.728	12.906	3.822	77.154
5	0.120	12	1.446	0.992	14	17.952	13.884	4.068	77.338
5	0.120	12	1.554	0.991	15	19.248	14.859	4.389	77.198
5	0.110	12	1.660	0.990	16	20.470	15.834	4.636	77.350
5	0.110	12	1.767	0.989	17	21.754	16.805	4.950	77.248
5	0.110	12	1.880	0.987	18	23.110	17.773	5.337	76.907
5	0.110	12	1.990	0.986	19	24.430	18.740	5.690	76.708
5	0.110	12	2.107	0.985	20	25.834	19.702	6.132	76.264
5	0.110	12	2.221	0.984	21	27.202	20.664	6.538	75.965
5	0.110	12	2.337	0.983	22	28.594	21.622	6.972	75.616
5	0.110	12	2.458	0.982	23	30.046	22.579	7.467	75.148
5	0.110	12	2.576	0.981	24	31.462	23.532	7.930	74.795
5	0.110	12	2.702	0.979	25	32.974	24.483	8.492	74.248
5	0.110	12	2.824	0.978	26	34.438	25.433	9.005	73.852
5	0.110	12	2.947	0.977	27	35.914	26.379	9.535	73.450
5	0.110	12	3.078	0.976	28	37.486	27.328	10.158	72.902
5	0.110	12	3.204	0.975	29	38.998	28.272	10.726	72.496
5	0.110	12	3.466	0.973	31	42.142	30.166	11.976	71.582
5	0.110	12	3.598	0.972	32	43.726	31.114	12.612	71.156
5	0.110	12	3.727	0.972	33	45.274	32.060	13.215	70.812
5	0.110	12	3.856	0.971	34	46.822	33.021	13.801	70.524
5	0.110	12	3.997	0.970	35	48.514	33.954	14.561	69.987

### Efficiency (Experimental Data with STS25NH3LL as a Bottom Switch)

Drivers		System				Calculation			
V <sub>D</sub> [V]	I <sub>D</sub> [A]	V <sub>IN</sub> [V]	I <sub>IN</sub> [A]	V <sub>O</sub> [A]	I <sub>O</sub> [A]	P <sub>IN</sub> [W]	P <sub>OUT</sub> [W]	P <sub>LOSS</sub> [W]	Efficiency [%]
5	0.09	12	0.06	1.006	0	1.17			
5	0.08	12	0.14	1.005	1	2.08	1.005	1.075	48.303
5	0.07	12	0.24	1.004	2	3.23	2.008	1.222	62.155
5	0.07	12	0.34	1.003	3	4.43	3.008	1.422	67.910
5	0.07	12	0.43	1.002	4	5.51	4.008	1.502	72.733
5	0.07	12	0.52	1.001	5	6.59	5.005	1.585	75.948
5	0.07	12	0.61	1.000	6	7.67	6.000	1.670	78.227
5	0.07	12	0.71	0.999	7	8.87	6.994	1.876	78.847
5	0.07	12	0.81	0.998	8	10.07	7.985	2.085	79.293
5	0.07	12	0.90	0.997	9	11.15	8.974	2.176	80.483
5	0.07	12	1.00	0.996	10	12.35	9.962	2.388	80.664
5	0.07	12	1.10	0.995	11	13.55	10.947	2.603	80.791
5	0.07	12	1.21	0.994	12	14.87	11.932	2.938	80.239
5	0.07	12	1.31	0.993	13	16.07	12.913	3.157	80.354
5	0.07	12	1.42	0.992	14	17.39	13.892	3.498	79.886
5	0.07	12	1.53	0.991	15	18.71	14.871	3.839	79.482
5	0.07	12	1.64	0.990	16	20.03	15.846	4.184	79.113
5	0.07	12	1.75	0.989	17	21.35	16.820	4.530	78.781
5	0.07	12	1.87	0.989	18	22.79	17.793	4.997	78.074
5	0.07	12	1.99	0.987	19	24.23	18.761	5.469	77.427
5	0.07	12	2.11	0.986	20	25.67	19.728	5.942	76.852
5	0.07	12	2.23	0.985	21	27.11	20.693	6.417	76.331
5	0.07	12	2.35	0.984	22	28.55	21.655	6.895	75.848
5	0.07	12	2.48	0.983	23	30.11	22.616	7.494	75.111
5	0.07	12	2.60	0.982	24	31.55	23.570	7.980	74.708
5	0.07	12	2.73	0.981	25	33.11	24.525	8.585	74.071
5	0.07	12	2.87	0.980	26	34.79	25.480	9.310	73.239
5	0.07	12	3.00	0.979	27	36.35	26.428	9.922	72.703
5	0.07	12	3.14	0.978	28	38.03	27.376	10.654	71.984
5	0.07	12	3.28	0.977	29	39.71	28.319	11.392	71.313
5	0.07	12	3.42	0.975	30	41.39	29.259	12.131	70.691
5	0.07	12	3.56	0.974	31	43.07	30.197	12.873	70.112
5	0.07	12	3.71	0.973	32	44.87	31.130	13.740	69.377
5	0.07	12	3.86	0.971	33	46.67	32.056	14.614	68.687
5	0.07	12	4.01	0.970	34	48.47	32.990	15.480	68.063
5	0.07	12	4.16	0.969	35	50.27	33.919	16.352	67.473
5	0.07	12	4.32	0.968	36	52.19	34.844	17.346	66.765
5	0.07	12	4.48	0.967	37	54.11	35.764	18.346	66.095
5	0.07	12	4.64	0.965	38	56.03	36.681	19.349	65.467
5	0.07	12	4.81	0.964	39	58.07	37.596	20.474	64.743
5	0.07	12	4.97	0.963	39.5	59.99	38.019	21.971	63.375

### Efficiency Data of Previous Board

Drivers		System				Calculations			
$V_{IN(DR)}$ [V]	$I_{IN(DR)}$ [A]	$V_{IN}$ [V]	$I_{IN}$ [A]	$V_{OUT}$ [V]	$I_{OUT}$ [A]	$P_{IN}$ [W]	$P_{OUT}$ [W]	$P_{LOSS}$ [W]	Efficiency [%]
5	0.10	12.04	0.20	1.006	1.03	2.91	1.04	1.87	35.739
5	0.10	12.03	0.31	1.006	2.02	4.23	2.03	2.20	47.991
5	0.10	12.02	0.42	1.006	3.03	5.55	3.05	2.50	54.955
5	0.10	12.00	0.54	1.006	4.03	6.98	4.05	2.93	58.023
5	0.09	11.98	0.65	1.006	5.00	8.24	5.03	3.21	61.044
5	0.10	11.98	0.78	1.006	6.03	9.84	6.07	3.78	61.687
5	0.09	11.96	0.90	1.006	7.02	11.22	7.06	4.16	62.923
5	0.09	11.95	1.03	1.006	8.03	12.76	8.08	4.68	63.323
5	0.09	11.94	1.16	1.006	9.01	14.29	9.06	5.23	63.401
5	0.09	11.92	1.29	1.006	10.02	15.83	10.08	5.75	63.677
5	0.09	11.91	1.42	1.006	11.03	17.36	11.10	6.26	63.940
5	0.09	11.89	1.56	1.006	12.02	19.00	12.09	6.91	63.632
5	0.09	11.88	1.70	1.006	13.01	20.64	13.09	7.55	63.421
5	0.09	11.86	1.84	1.006	14.00	22.27	14.09	8.19	63.269
5	0.09	11.84	1.99	1.006	15.00	24.02	15.09	8.93	62.823
5	0.09	11.83	2.14	1.006	16.02	25.76	16.12	9.64	62.578
5	0.09	11.81	2.28	1.006	17.00	27.38	17.10	10.28	62.454
5	0.09	11.80	2.44	1.006	18.01	29.23	18.12	11.11	61.991
5	0.09	11.78	2.59	1.006	19.00	30.96	19.12	11.84	61.757
5	0.09	11.76	2.74	1.006	20.01	32.68	20.13	12.54	61.597
5	0.10	12.26	3.01	1.006	22.00	37.41	22.13	15.28	59.155
5	0.10	11.99	3.43	1.006	24.00	41.61	24.14	17.47	58.015
5	0.10	12.16	3.70	1.006	26.00	45.49	26.15	19.34	57.485
5	0.10	12.11	4.06	1.006	28.01	49.66	28.18	21.48	56.746
5	0.10	12.05	4.42	1.006	30.01	53.78	30.19	23.59	56.136
5	0.10	11.99	4.85	1.006	32.01	58.66	32.20	26.46	54.893
5	0.10	11.95	5.12	1.006	34.00	61.67	34.21	27.46	55.473
5	0.10	12.09	5.47	1.006	36.00	66.62	36.22	30.40	54.368
5	0.10	12.03	5.83	1.006	38.00	70.64	38.24	32.41	54.134

## Power Loss Calculations in Converter

$V_{IN}$ [V]	12
$V_O$ [V]	1
$D_1$	0.083333333
$D_2$	0.166666667
$D_3$	0.333333333
$I_1$ [A]	10
$I_2$ [A]	20
$I_3$ [A]	40
$f_1$ [Hz]	500000
$f_2$ [Hz]	1000000
$f_3$ [Hz]	2000000
DCR [ $\Omega$ ]	0.00074
$i_{C3} = \Delta I_{L1}/\sqrt{3}$ [A]	0.577350269
$i_{C1} = \Delta I_{L2}/\sqrt{3}$ [A]	0.288675135
$i_{C0} = \Delta I_{L3}/\sqrt{3}$ [A]	0.144337567
ESR [ $\Omega$ ]	0.01
$\Delta I_{L1}$ [A]	1
$\Delta I_{L2}$ [A]	0.5
$\Delta I_{L3}$ [A]	0.25
$V_{G1}$ [V]	10
$V_{G2}$ [V]	5
$I_{RMS,H}$ [A]	2.891558595
$I_{RMS,L}$ [A]	9.590214921
$L_1 = V_O (1-D)T / (\Delta I_L * f_1)$ [H]	1.83333E-06
$L_5 = V_O (1-D)T / (\Delta I_L * f_2)$ [H]	1.66667E-06
$L_7 = V_O (1-D)T / (\Delta I_L * f_2)$ [H]	1.66667E-06
$C_3 = i_{C3} * DT / \Delta V$ [F]	9.6225E-08
$C_1 = i_{C1} * DT / \Delta V$ [F]	4.37387E-09
$C_0 = (1-D)V / 8Lf^2 \Delta V$ [F]	0.00000125

Power Loss [W]	Total Power Loss [W]
0.074	0.296
0.296	0.592
0.296	0.592
0.003333333	0.006666667
0.000833333	0.001666667
0.000208333	0.000208333
<b>Cummulative Loss [W]</b>	<b>1.488541667</b>